```
=> fil hcaplus
FILE 'HCAPLUS' ENTERED AT 11:12:52 ON 09 MAR 2009
USE IS SUBJECT TO THE TERMS OF YOUR STN CUSTOMER AGREEMENT.
PLEASE SEE "HELP USAGETERMS" FOR DETAILS.
COPYRIGHT (C) 2009 AMERICAN CHEMICAL SOCIETY (ACS)
```


FILE COVERS 1907 - 9 Mar 2009 VOL 150 ISS 11
FILE LAST UPDATED: 8 Mar 2009 (20090308/ED)

HCAplus now includes complete International Patent Classification (IPC) reclassification data for the third quarter of 2008.

CAS Information Use Policies apply and are available at:

http://www.cas.org/legal/infopolicy.html

This file contains CAS Registry Numbers for easy and accurate substance identification.

```
=> d l175 bib abs hitind hitstr tot

L175 ANSWER 1 OF 5  HCAPLUS  COPYRIGHT 2009 ACS on STN
AN   2005:371521  HCAPLUS  Full-text
DN   142:402393
TI   Composition for forming silicon-cobalt film, for SALICIDE gate contacts in
     MOS transistor integrated circuit fabrication
IN   Matsuki, Yasuo; Wang, Daohai; Sakai, Tatsuya
     ; Iwasawa, Haruo
PA   JSR Corporation, Japan
SO   PCT Int. Appl., 27 pp.
     CODEN: PIXXD2
DT   Patent
LA   Japanese
FAN.CNT 1
     PATENT NO.          KIND   DATE        APPLICATION NO.        DATE
     ---------------     ----   --------    -------------------    --------
PI   WO 2005038891        A1    20050428    WO 2004-JP15101        20041006 <--
         W:  AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH,
             CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD,
             GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC,
             LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI,
             NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY,
             TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW
         RW: BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW, AM,
             AZ, BY, KG, KZ, MD, RU, TJ, TM, AT, BE, BG, CH, CY, CZ, DE, DK,
             EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE,
             SI, SK, TR, BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE,
             SN, TD, TG
```

	JP 2005142540	A	20050602	JP 2004-293581	20041006 <--
	CN 1868037	A	20061122	CN 2004-80030494	20041006 <--
	CN 100423199	C	20081001		
	US 20070077742	A1	20070405	US 2006-575478	20060412 <--
	KR 2007017966	A	20070213	KR 2006-707169	20060414 <--
PRAI	JP 2003-356158	A	20031016 <--		
	WO 2004-JP15101	W	20041006 <--		

AB The invention relates to a composition and a method for forming a silicon-cobalt film at low production cost without requiring an expensive vacuum apparatus or high-frequency wave generating apparatus A composition for forming a silicon-cobalt film contains a silicon compound and a cobalt compound A silicon-cobalt film is formed by applying this composition to a base and treating it with heat or light.

IC ICM H01L0021-28
ICS H01L0021-288; B05D0003-00; B32B0015-01; C01B0033-04; C07F0017-02

CC 76-3 (Electric Phenomena)

IT 50955-74-3
RL: DEV (Device component use); EPR (Engineering process); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(Co-Si film forming composition for SALICIDE gate contact in MOS transistor integrated circuit fabrication)

IT 50955-74-3
RL: DEV (Device component use); EPR (Engineering process); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(Co-Si film forming composition for SALICIDE gate contact in MOS transistor integrated circuit fabrication)

RN 50955-74-3 HCAPLUS

CN Cobalt alloy, nonbase, Co,Si (CA INDEX NAME)

Component	Component Registry Number
Co	7440-48-4
Si	7440-21-3

RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L175 ANSWER 2 OF 5 HCAPLUS COPYRIGHT 2009 ACS on STN

AN 2001:713853 HCAPLUS Full-text

DN 135:250417

TI Method for manufacturing a gate structure incorporating therein aluminum oxide as a gate dielectric to reduce leakage current and lower interface state density

IN Park, Dae-Gyu; Jang, Se-Aug; Lee, Jeong-youb

PA Hyundai Electronics Industries Co., Ltd., S. Korea

SO U.S. Pat. Appl. Publ., 6 pp.
CODEN: USXXCO

DT Patent

LA English

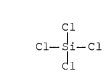
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 20010024860	A1	20010927	US 2000-739292	20001219 <--
	US 6524918	B2	20030225		
	KR 2001065161	A	20010711	KR 1999-65030	19991229 <--
PRAI	KR 1999-65030	A	19991229 <--		

AB A method for forming a gate structure begins by preparing a semiconductor substrate provided with an isolation region formed therein. An Al2O3 layer is deposited on top of the semiconductor substrate and then, Si ion plasma doping

is carried out. Thereafter, the Al2O3 layer doped with Si ions is annealed in the presence of O gas or nitrous oxide to remove a metallic vacancy in the Al2O3 layer. Subsequently, a conductive layer is formed on top of the Al2O3 layer. Finally, the conductive layer is patterned into the gate structure.

IC ICM H01L0021-336
ICS H01L0021-3205; H01L0021-4763
INCL 438287000
CC 76-3 (Electric Phenomena)
IT Annealing
Lithography
(in method for manufacturing gate structure incorporating therein aluminum oxide as gate dielec. to reduce leakage current and lower interface state d.)
IT Coating process
Gate contacts
Oxidation
(method for manufacturing gate structure incorporating therein aluminum oxide
as gate dielec. to reduce leakage current and lower interface state d.)
IT 75-24-1, Trimethylaluminum 1184-58-3, Dimethylaluminum chloride
1590-87-0, Silicon hydride (Si2H6) 7446-70-0, Aluminum trichloride, uses
7727-37-9, Nitrogen, uses 7732-18-5, Water, uses 7782-39-0, Deuterium, uses 7803-62-5, Silicon hydride (SiH4), uses 10026-04-7, Silicon chloride (SiCl4) 10028-15-6, Ozone, uses
RL: NUU (Other use, unclassified); USES (Uses)
(in method for manufacturing gate structure incorporating therein aluminum oxide as gate dielec. to reduce leakage current and lower interface state d.)
IT 7440-33-7, Tungsten, processes 7631-86-9, Silica, processes
11104-62-4, Cobalt silicide 11104-85-1, Molybdenum silicide
12033-62-4, Tantalum nitride (TaN) 12058-38-7, Tungsten nitride (WN)
12627-41-7, Tungsten silicide 25583-20-4, Titanium nitride (TiN)
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(in method for manufacturing gate structure incorporating therein aluminum oxide as gate dielec. to reduce leakage current and lower interface state d.)
IT 10026-04-7, Silicon chloride (SiCl4)
RL: NUU (Other use, unclassified); USES (Uses)
(in method for manufacturing gate structure incorporating therein aluminum oxide as gate dielec. to reduce leakage current and lower interface state d.)
RN 10026-04-7 HCAPLUS
CN Silane, tetrachloro- (CA INDEX NAME)



IT 11104-62-4, Cobalt silicide
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(in method for manufacturing gate structure incorporating therein aluminum oxide as gate dielec. to reduce leakage current and lower interface state d.)
RN 11104-62-4 HCAPLUS

CN Cobalt silicide (CA INDEX NAME)

Component	Ratio	Component Registry Number
Co	x	7440-48-4
Si	x	7440-21-3

L175 ANSWER 3 OF 5 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 2001:25721 HCAPLUS Full-text
DN 134:94240
TI Method for forming self-aligned silicided MOS transistors with electrostatic discharge protection improvement
IN Wu, Shye-Lin
PA Texas Instruments - Acer Incorporated, Taiwan
SO U.S., 10 pp., Cont.-in-part of U. S. 6,022,769.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6171893	B1	20010109	US 1999-366606	19990803 <--
US 6022769	A	20000208	US 1997-996694	19971223 <--
PRAI US 1997-996694	A2	19971223 <--		

AB The method of forming MOS transistors includes the following steps. First, isolation regions are formed in the semiconductor substrate to sep. the semiconductor substrate into an ESD protective region and a functional region. A gate insulator layer is formed on the substrate and a polysilicon layer is formed on the gate insulator layer. The polysilicon layer is then patterned to form gate structures on the ESD protective region and the functional region. The semiconductor substrate is doped for forming a 1st doped region and an insulator layer is formed over the semiconductor substrate. A portion of the insulator layer and a portion of the gate insulator layer are removed to form spacer structures and an insulator block. The semiconductor substrate is doped for forming a 2nd doped region. An insulator opening is defined within the insulator block. The semiconductor substrate is then doped for forming a 3rd doped region. In the preferred embodiments, the 3rd doped region has opposite type dopants with the 2nd doped region and the 1st doped region. A 1st thermal annealing is then performed to the semiconductor substrate to drive in dopants. A metal layer is then formed on the semiconductor substrate and a 2nd thermal annealing is performed to the semiconductor substrate to form a metal silicide layer on the gate structures, and on the substrate over the 2nd doped region and the 3rd doped region. Finally, unreacted portions of the metal layer are removed.
IC ICM H01L0021-8238
INCL 438200000
CC 76-3 (Electric Phenomena)
IT Annealing
Dielectric films
Doping
Ion implantation
MOS transistors
Semiconductor device fabrication
(method for forming self-aligned silicided MOS transistors with electrostatic discharge protection improvement)
IT 75-37-6, 1,1-Difluoroethane 75-46-7, Trifluoromethane 75-71-8, Dichlorodifluoromethane 75-73-0, Carbon tetrafluoride (CF4) 1336-21-6, Ammonium hydroxide 2551-62-4 7722-84-1, Hydrogen peroxide, processes

7726-95-6, Bromine, processes 7782-50-5, Chlorine, processes 10026-04-7, Silicon chloride (SiCl4) 10035-10-6, Hydrogen bromide, processes 10294-34-5
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(etchant; method for forming self-aligned silicided MOS transistors with electrostatic discharge protection improvement)

IT 7440-02-0, Nickel, uses 7440-06-4, Platinum, uses 7440-32-6, Titanium, uses 7440-33-7, Tungsten, uses 7440-48-4, Cobalt, uses
RL: DEV (Device component use); USES (Uses)
(semiconductor device metal layer; method for forming self-aligned silicided MOS transistors with electrostatic discharge protection improvement)

IT 10026-04-7, Silicon chloride (SiCl4)
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(etchant; method for forming self-aligned silicided MOS transistors with electrostatic discharge protection improvement)

RN 10026-04-7 HCAPLUS
CN Silane, tetrachloro- (CA INDEX NAME)

IT 7440-48-4, Cobalt, uses
RL: DEV (Device component use); USES (Uses)
(semiconductor device metal layer; method for forming self-aligned silicided MOS transistors with electrostatic discharge protection improvement)

RN 7440-48-4 HCAPLUS
CN Cobalt (CA INDEX NAME)

RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L175 ANSWER 4 OF 5 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 2000:547433 HCAPLUS Full-text
DN 133:128714
TI Self-aligned silicided MOS transistor with a lightly doped drain ballast resistor for ESD protection
IN Wu, Shye-Lin
PA Texas Instruments - Acer Incorporated, Taiwan
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6100127	A	20000808	US 1997-990167	19971212 <--

PRAI US 1997-990167 19971212 <--

AB A MOS transistor with a self-aligned silicide and a lightly doped drain ballast resistor for ESD protection on a semiconductor substrate is formed with the method in the present invention. The ESD protection devices in a ESD protective region are formed at the same time with the forming of the NMOS, PMOS, or both in a functional region. The transistors with a lightly doped drain (LDD) structure and an ultra-shallow junction can be manufactured The short channel effect and it's accompanying hot carrier effect is eliminated. ESD damage from external connections to the integrated circuits are kept from the densely packed devices. The self-aligned silicide (salicide) technol. employed in the present invention for forming low resistance contacts provides high operation speed with low heat generation. Integrated circuits with ESD hardness and high circuit operation speed of the functional devices are provided by the semiconductor manufacturing process employing the method disclosed.

IC ICM H01L0021-8234
ICS H01L0021-336

INCL 438238000

CC 76-3 (Electric Phenomena)

IT Integrated circuits
MOS transistors
Resistors
Semiconductor device fabrication
(self-aligned silicided MOS transistor with lightly doped drain ballast resistor for ESD protection and its fabrication)

IT Annealing
Dielectric films
Doping
Electric activation (dopants)
Ion implantation
Photolithography
Siliconizing
(self-aligned silicided MOS transistor with lightly doped drain ballast resistor for ESD protection and its fabrication using)

IT 75-73-0, Carbon tetrafluoride 2551-62-4, Sulfur hexafluoride 7726-95-6, Bromine, uses 7782-44-7, Oxygen, uses 7782-50-5, Chlorine, uses 10026-04-7, Tetrachlorosilane 10035-10-6, Hydrogen bromide, uses 10294-34-5, Boron trichloride
RL: NUU (Other use, unclassified); USES (Uses)
(polysilicon etchant; self-aligned silicided MOS transistor with lightly doped drain ballast resistor for ESD protection and its fabrication using)

IT 7440-06-4, Platinum, processes 7440-32-6, Titanium, processes 7440-33-7, Tungsten, processes 7440-48-4, Cobalt, processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(silicidation precursor; self-aligned silicided MOS transistor with lightly doped drain ballast resistor for ESD protection and its fabrication using)

IT 10026-04-7, Tetrachlorosilane
RL: NUU (Other use, unclassified); USES (Uses)
(polysilicon etchant; self-aligned silicided MOS transistor with lightly doped drain ballast resistor for ESD protection and its fabrication using)

RN 10026-04-7 HCAPLUS

CN Silane, tetrachloro- (CA INDEX NAME)

IT 7440-48-4, Cobalt, processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(silicidation precursor; self-aligned silicided MOS transistor with lightly doped drain ballast resistor for ESD protection and its fabrication using)
RN 7440-48-4 HCAPLUS
CN Cobalt (CA INDEX NAME)

RE.CNT 13 THERE ARE 13 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L175 ANSWER 5 OF 5 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 1993:39134 HCAPLUS Full-text
DN 118:39134
OREF 118:7139a,7142a
TI Cobalt carbonyl complexes from alkynylsilanes
AU Lang, Heinrich; Lay, Uwe; Weinmann, Markus
CS Anorg. Chem. Inst., Univ. Heidelberg, Heidelberg, W-69001, Germany
SO Journal of Organometallic Chemistry (1992), 436(3), 265-76
CODEN: JORCAI; ISSN: 0022-328X
DT Journal
LA German
OS CASREACT 118:39134
AB Reaction of the phenylethynyl-substituted silanes RR1SiHC.tplbond.CPh (I-III, XXII) and PhC.tplbond.CSiH2R (XII, XIII) with Co2(CO)8 gives monomeric and oligomeric complex compds. Co2(CO)8 (IV) reacts selectively with RR1SiHC.tplbond.CPh [R = Me, R1 = Et (I), C.tplbond.CPh (II); R, R1 = C.tplbond.CPh (III)] or PhC.tplbond.CSiH2R [R = Ph (XII), C.tplbond.CPh (XIII)] to yield the dinuclear complexes [(η2-C.tplbond.CPh)Co2(CO)6]SiHRR1 (V-VII, XIV and XV, resp.). In these compds. 1 of the phenylethynyl groups is η2-side-on coordinated to Co2(CO)6, forming space-filling dicobaltatetrahedrane units. V and XIV react with 0.5 equiv Co2(CO)8 via SiH-substitution to yield [(η2-C.tplbond.CPh)Co2(CO)6][Co(CO)4]SiRR1 (VIII and XVII, resp.). VI, VII, and XV each contain addnl. noncoordinated C.tplbond.CPh units, and afford with IV [(η2-C.tplbond.CPh)Co2(CO)6]2SiHR [R = Me (IX), C.tplbond.CPh (X), H (XVI)]. X reacts with further Co2(CO)8 to yield [(η2-C.tplbond.CPh)Co2(CO)6]3SiH (XI); XI was also synthesized from VII and 2 equiv IV. VIII, IX, XI, XVI, and XVII were also obtained directly from I, III, VII, and VIII, resp. An alternative route to XVII is given in the reaction sequence PhC.tplbond.CSiCl2Ph (XVIII) → XIX → XXI → XVII; XVIII with IV yields the dinuclear compound [(η2-C.tplbond.CPh)Co2(CO)6]SiCl2Ph (XIX). XIX reacts with Na[Co(CO)4] (XX) affording [(η2-C.tplbond.CPh)Co2(CO)6][Co(CO)4]SiClPh (XXI). Reduction of XXI with LiAlH4 yields XVII. Reaction of CH2:CHSiHPhC.tplbond.CPh with equimolar amts. of IV affords an oligomer of the idealized composition [Me[η2-

C.tplbond.CPh)Co2(CO)6]SiCH2CH2]n. All new synthesized compds. were characterized by anal. and spectroscopic data (IR, 1H and 13C NMR, MS).

CC 29-13 (Organometallic and Organometalloidal Compounds)

IT 129469-56-3P 136910-05-9P 145175-45-7P 145175-46-8P 145175-47-9P 145175-48-0P 145175-49-1P 145175-52-6P 145227-74-3P 145227-75-4P 145312-74-9P 145312-77-2P
RL: SPN (Synthetic preparation); PREP (Preparation)
(preparation of)

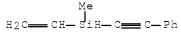
IT 145312-77-2P
RL: SPN (Synthetic preparation); PREP (Preparation)
(preparation of)

RN 145312-77-2 HCAPLUS

CN Cobalt, di-μ-carbonylhexacarbonyldi-, (Co-Co), polymer with ethenylmethyl(phenylethynyl)silane (9CI) (CA INDEX NAME)

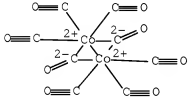
CM 1

CRN 136910-05-9
CMF C11 H12 Si



CM 2

CRN 10210-68-1
CMF C8 Co2 O8
CCI CCS



=> => d his

(FILE 'HOME' ENTERED AT 09:38:51 ON 09 MAR 2009)
SET COST OFF

FILE 'HCAPLUS' ENTERED AT 09:39:04 ON 09 MAR 2009
L1 1 S US20070077742/PN OR (US2006-575478# OR WO2004-JP15101 OR JP20
E MATSUKI/AU
L2 1 S E3
E MATSUKI Y/AU
L3 291 S E3,E9
E MATSUKI NAME/AU
L4 4 S E4

```
                E Y ASUO/AU
                E YASUO/AU
L5            1 S E3
                E YASUO M/AU
L6            3 S E3
                E WANG/AU
L7           16 S E3
                E WANG D/AU
L8          929 S E3,E12
                E WANG DAO/AU
L9           69 S E3,E12
                E WANG DAOHAI/AU
L10          11 S E3
                E WANG NAME/AU
L11         114 S E4
                E DAO/AU
                E DAO H/AU
L12           7 S E3
                E DAO NAME/AU
                E DAOHAI/AU
                E SAKAI/AU
                E SAKAI T/AU
L13        1180 S E3
                E SAKAI TAT/AU
L14          86 S E18
                E SAKAI NAME/AU
L15          74 S E4
                E TATSUYA/AU
L16           2 S E3
                E TATSUYA S/AU
                E TATSUYA NAME/AU
                E IWASAWA/AU
                E IWASAWA H/AU
L17          82 S E3,E5
                E IWASAWA NAME/AU
L18           1 S E4
                E HARUO/AU
L19           2 S E3
                E JSR/CO
L20        4757 S E3-E29/CO,PA,CS
                E E8+ALL
L21       10518 S E2+RT OR E30-E32 OR E2-E32/PA,CS
L22           1 S L1 AND L2-L21
                SEL RN

     FILE 'REGISTRY' ENTERED AT 09:43:47 ON 09 MAR 2009
L23           1 S E1
L24       47583 S (7440-21-3/CRN OR SI/ELS OR SILICON) AND (7440-48-4/CRN OR CO
L25       42886 S L24 AND (TIS OR AYS)/CI
L26         170 S L25 AND 2/ELC.SUB
L27         170 S L23,L26
L28        4697 S L24 NOT L25

     FILE 'HCAPLUS' ENTERED AT 09:45:29 ON 09 MAR 2009
L29           5 S N PENTASILANE
L30         181 S PENTASILANE
L31           5 S ISOPENTASILANE OR ISO PENTASILANE
L32          16 S NEOPENTASILANE OR NEO PENTASILANE
L33           2 S N HEXASILANE
L34         164 S HEXASILANE
```

```
L35          55 S N HEPTASILANE OR HEPTASILANE
L36          82 S N OCTASILANE OR OCTASILANE
L37          14 S N NONASILANE OR NONASILANE
L38        2542 S TETRACHLOROSILANE OR TETRACHLORO SILANE OR TETRA CHLOROSILANE
L39          78 S TETRABROMOSILANE OR TETRABROMO SILANE OR TETRA BROMOSILANE OR
L40         464 S HEXACHLORODISILANE OR HEXACHLORO DISILANE OR HEXA CHLORODISIL
L41          12 S HEXABROMODISILANE OR HEXABROMO DISILANE OR HEXA BROMODISILANE
L42          36 S OCTACHLOROTRISILANE OR OCTACHLORO TRISILANE OR OCTA CHLOROTRI
L43           0 S OCTABROMOTRISILANE OR OCTABROMO TRISILANE OR OCTA BROMOTRISIL
L44         135 S CYCLOTRISILANE
L45         183 S CYCLOTETRASILANE
L46         165 S CYCLOPENTASILANE
L47           0 S SILYLCYCLOTETRASILANE
L48           0 S SILYL CYCLOTETRASILANE
L49           0 S SILYL CYCLO TETRASILANE
L50           0 S SILYLCYCLOTRISILANE
L51          14 S SILYLCYCLOPENTASILANE
L52         181 S CYCLOHEXASILANE
L53           6 S CYCLOHEPTASILANE
L54           3 S CYCLOOCTASILANE
L55           0 S 1 1 BICYCLOBUTASILANE
L56           0 S BICYCLOBUTASILANE
L57           4 S BICYCLOPENTASILANE OR 1 1 BICYCLOPENTASILANE
L58           9 S 1 1 BICYCLOHEXASILANE OR BICYCLOHEXASILANE
L59           2 S 1 1 BICYCLOHEPTASILANE OR BICYCLOHEPTASILANE
L60           0 S 1 1 CYCLOBUTASILYLCYCLOPENTASILANE
L61           0 S CYCLOBUTASILYLCYCLOPENTASILANE
L62           0 S CYCLOBUTASILYLCYCLOHEXASILANE OR CYCLOBUTASILYLCYCLOHEPTASILA
L63           1 S SPIRO 2 2 PENTASILANE
L64           1 S SPIRO 3 3 HEPTASILANE
L65           0 S SPIRO 4 4 NONAASILANE
L66           0 S SPIRO 4 5 DECASILANE
L67           0 S SPRIO 4 6 UNDECASILANE
L68           0 S SPIRO 5 5 UNDECASILANE
L69           0 S SPIRO 5 6 UNDECASILANE
L70           0 S SPIRO 6 6 TRIDECASILANE
L71          54 S HEXASILAPRISMANE OR OCTASILACUBANE

     FILE 'REGISTRY' ENTERED AT 10:02:40 ON 09 MAR 2009
L72          18 S 39517-09-4 OR 18839-38-8 OR 10026-04-7 OR 7789-66-4 OR 13465-
L73           7 S 101753-14-4 OR 291-59-8 OR 15691-01-7 OR 168294-11-9 OR 29920
L74          25 S L72,L73
L75           1 S L74 AND C100H92SI9
L76           1 S L74 AND C16H48SI8
L77          23 S L74 NOT L75,L76
                E NONASILANE/CN
L78           1 S E3
                E OCTABROMOTRISILANE/CN
                E BR8SI3/MF
L79           1 S E3
                E CYCLOTETRASILANE, SILYL-/CN
L80           1 S E3
                E CYCLOTRISILANE, SILYL-/CN
L81           1 S E3
                E CYCLOOCTASILANE/CN
L82           1 S E3
                E "1,1'-BICYCLOBUTASILANE"/CN
                E "1,1'-BICYCLOTETRASILANE"/CN
L83           1 S L77 AND SI4/ES
                E H14SI8/MF
```

```
L84           2 S 4.859/RID AND 2/NR AND 2/ELC.SUB
L85           1 S L84 AND 869812-46-4
                E "1,1'-BICYCLOHEPTASILANE"/CN
L86           1 S L77 AND SI7/ES
                E "SPIRO[4.4]NONASILANE"/CN
                E "SPIRO(4.4)NONASILANE"/CN
L87           1 S E3
                E "SPIRO(4.5)DECASILANE"/CN
                E "SPIRO(4.6)UNDECASILANE"/CN
                E "SPIRO(5.5)UNDECASILANE"/CN
                E "SPIRO(5.6)UNDECASILANE"/CN
                E "SPIRO(6.6)TRIDECASILANE"/CN
                E "1,1'-CYCLOHEXASILYLCYCLOHEPTASILANE"/CN
L88          30 S L77-L83,L85-L87

     FILE 'HCAPLUS' ENTERED AT 10:24:03 ON 09 MAR 2009
L89       12300 S L88
L90         219 S L89 AND COBALT
L91          20 S CYCLOPENTADIENYL DICARBONYL COBALT
L92          13 S DICARBONYLCYCLOPENTADIENYL COBALT
L93          80 S BIS CYCLOPENTADIENYL COBALT
L94         107 S OCTACARBONYL DICOBALT

     FILE 'REGISTRY' ENTERED AT 10:26:02 ON 09 MAR 2009
L95           3 S 12078-25-0 OR 1277-43-6 OR 10210-68-1
L96         110 S (12078-25-0 OR 1277-43-6 OR 10210-68-1)/CRN
L97           1 S L96 AND SI/ELS

     FILE 'HCAPLUS' ENTERED AT 10:26:48 ON 09 MAR 2009
L98           1 S L97
L99          14 S L95,L91-L94 AND L89
L100         82 S L1-L22 AND L89
L101         56 S L1-L22 AND L29-L71
L102         89 S L100,L101
L103          1 S L102 AND ?COBALT?
L104        313 S L90,L98,L99,L102,L103

     FILE 'REGISTRY' ENTERED AT 10:30:13 ON 09 MAR 2009

     FILE 'HCAPLUS' ENTERED AT 10:30:13 ON 09 MAR 2009
L105            TRA L104 1- RN :     5273 TERMS

     FILE 'REGISTRY' ENTERED AT 10:30:31 ON 09 MAR 2009
L106       5273 SEA L105
L107        215 S L106 AND CO/ELS
L108        215 S L106 AND ?COBALT?/CNS
L109         39 S L106 AND 7440-48-4/CRN
L110        216 S L107-L109
L111          2 S L110 AND L27
L112         12 S L110 AND (C12CO4O12 OR C9H13CO OR C10H14COO4 OR C12CO4O12 OR
L113         11 S L112 NOT SI/ELS
L114          1 S L112 NOT L113
L115          1 S L97,L114
L116        544 S L106 AND SI/ELS
L117         15 S L106 AND L88
L118          2 S L116 AND L27
L119        473 S L116 NOT L110,L117,L118
L120        388 S L119 NOT (CCS OR PMS OR MXS OR MAN)/CI
L121        307 S L120 NOT (TIS OR AYS)/CI
L122        256 S L121 NOT (N OR B OR P OR S)/ELS
```

```
L123          3 S (CYCLOPENTASILANE OR CYCLOTETRASILANE OR CYCLOTRISILANE)/CN
L124          3 S L88 AND SI5/ES
L125          3 S L88 AND SI4/ES
L126          2 S L88 AND SI3/ES
L127          5 S L124-L126 NOT L123
                SEL RN 2 3 5
L128          3 S E1-E3
L129          6 S L123,L128

     FILE 'HCAPLUS' ENTERED AT 11:00:41 ON 09 MAR 2009
L130        195 S L129
L131         81 S L130 AND PY<=2003 NOT P/DT
L132         74 S L130 AND (PY<=2003 OR PRY<=2003 OR AY<=2003) AND P/DT
L133        155 S L131,L132
L134          0 S L133 AND ?COBALT?

     FILE 'REGISTRY' ENTERED AT 11:01:32 ON 09 MAR 2009

     FILE 'HCAPLUS' ENTERED AT 11:01:32 ON 09 MAR 2009
L135            TRA L133 1- RN :      766 TERMS

     FILE 'REGISTRY' ENTERED AT 11:01:37 ON 09 MAR 2009
L136        766 SEA L135
L137          0 S L136 AND (?COBALT?/CNS OR CO/ELS OR 7440-48-4/CRN OR 7440-48-

     FILE 'HCAPLUS' ENTERED AT 11:02:54 ON 09 MAR 2009
L138       3099 S L27
L139        739 S L138 AND PY<=2003 NOT P/DT
L140       1359 S L138 AND (PY<=2003 OR PRY<=2003 OR AY<=2003) AND P/DT
L141       2098 S L139,L140
L142        277 S L141 AND INTEGRATED CIRCUITS+OLD,NT/CT
L143         29 S L141 AND IC
L144        308 S L141 AND INTEGRATED CIRCUIT
L145        907 S L141 AND ?FILM?
L146        144 S L145 AND L142-L144
L147          1 S L146 AND LIGHT
L148         20 S L146 AND HEAT
L149          1 S L146 AND UV RADIATION+OLD,NT/CT
L150         55 S L146 AND MOS TRANSISTORS+OLD,NT/CT
L151         10 S L147-L149 AND L150
L152         32 S L146 AND GATE CONTACTS+OLD,NT/CT
L153          5 S L152 AND L147-L149
L154         11 S L151,L153
L155          1 S L1-L22 AND L138
L156         11 S L154,L155
L157         92 S L144 AND HEAT TREATMENT+OLD,NT/CT
L158         26 S L157 AND L147,L149,L150,L152
L159         10 S L156 AND L158
L160         11 S L156,L159
L161       5283 S L89 AND PY<=2003 NOT P/DT
L162       5334 S L89 AND (PY<=2003 OR PRY<=2003 OR AY<=2003) AND P/DT
L163      10617 S L161,L162
L164        164 S L163 AND (INTEGRATED CIRCUITS+OLD,NT/CT  OR IC OR INTEGRAT? C
L165         27 S L163 AND UV RADIATION+OLD,NT/CT
L166        119 S L163 AND HEAT TREATMENT+OLD,NT/CT
L167       1085 S L163 AND (LIGHT OR HEAT)
L168         26 S L164 AND L165-L167

     FILE 'REGISTRY' ENTERED AT 11:10:25 ON 09 MAR 2009
```

```
     FILE 'HCAPLUS' ENTERED AT 11:10:25 ON 09 MAR 2009
L169            TRA L168 1- RN :      154 TERMS

     FILE 'REGISTRY' ENTERED AT 11:10:27 ON 09 MAR 2009
L170        154 SEA L169
L171          2 S L170 AND (CO/ELS OR COBALT OR 7440-48-4/CRN OR 7440-48-4)

     FILE 'HCAPLUS' ENTERED AT 11:11:08 ON 09 MAR 2009
L172          3 S L171 AND L168
L173          1 S L1-L22 AND L141
L174          4 S L172,L173
L175          5 S L174,L98

     FILE 'HCAPLUS' ENTERED AT 11:12:52 ON 09 MAR 2009

=> => d bib abs hitind hitstr tot

L95  ANSWER 1 OF 28  HCAPLUS  COPYRIGHT 2009 ACS on STN
AN   2008:1310089  HCAPLUS  Full-text
DN   149:523110
TI   Process for forming cobalt and cobalt silicide
     materials in copper contact applications
IN   Yu, Sang-Ho; Moraes, Kevin Ti; Ganguli, Seshadri; Chung, Hua; Phan,
     See-Eng; Khandelwal, Amit; Wu, Kai
PA   USA
SO   U.S. Pat. Appl. Publ., 63pp., Cont.-in-part of U.S. Ser. No. 733,929.
     CODEN: USXXCO
DT   Patent
LA   English
FAN.CNT 6
     PATENT NO.          KIND   DATE        APPLICATION NO.        DATE
     ----------          ----   --------    -------------------    --------
PI   US 20080268635      A1     20081030    US 2008-111930         20080429 <--
     US 20030029715      A1     20030213    US 2001-916234         20010725 <--
     US 20030022487      A1     20030130    US 2002-44412          20020109 <--
     US 6740585          B2     20040525
     US 20040211665      A1     20041028    US 2004-845970         20040514 <--
     US 20060276020      A1     20061207    US 2006-456073         20060706 <--
     US 7416979          B2     20080826
     US 20070202254      A1     20070830    US 2007-733929         20070411 <--
     WO 2007121249       A2     20071025    WO 2007-US66442        20070411
     WO 2007121249       A3     20071227
         W:  AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA,
             CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB,
             GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM,
             KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, MG, MK,
             MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO,
             RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT,
             TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW
         RW: AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE,
             IS, IT, LT, LU, LV, MC, MT, NL, PL, PT, RO, SE, SI, SK, TR, BF,
             BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG, BW,
             GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW, AM, AZ,
             BY, KG, KZ, MD, RU, TJ, TM, AP, EA, EP, OA
     US 20090053426      A1     20090226    US 2008-201976         20080829 <--
     KR 2008110897       A      20081219    KR 2008-727610         20081111
PRAI US 2001-916234      A2     20010725  <--
     US 2002-44412       A1     20020109  <--
     US 2004-845970      A1     20040514
     US 2006-791366P     P      20060411
```

US 2006-456073 A2 20060706
US 2006-863939P P 20061101
US 2007-733929 A2 20070411
WO 2007-US66442 W 20070411
US 2008-111923 A2 20080429
US 2008-111930 A2 20080429

AB Embodiments of the invention described herein generally provide methods for forming cobalt silicide layers and metallic cobalt layers by using various deposition processes and annealing processes. In one embodiment, a method for forming a cobalt silicide material on a substrate is provided which includes treating the substrate with at least one preclean process to expose a silicon-containing surface, depositing a cobalt silicide material over the silicon-containing surface, and depositing a copper material over the cobalt silicide material. In another embodiment, a metallic cobalt material may be deposited over the cobalt silicide material prior to depositing the copper material. In one example, the copper material may be formed by depositing a copper seed layer and a copper bulk layer on the substrate. The copper seed layer may be deposited by a PVD process and the copper bulk layer may be deposited by an ECP process or an electroless deposition process.

INCL 438655000; 257-E21.476
CC 76-3 (Electric Phenomena)

ST cobalt silicide material copper contact application deposition annealing

IT Polishing
(chemical-mech.; process for forming cobalt and cobalt silicide materials in copper contact applications)

IT Vapor deposition process
(chemical; process for forming cobalt and cobalt silicide materials in copper contact applications)

IT Coating process
(electroless; process for forming cobalt and cobalt silicide materials in copper contact applications)

IT Annealing
Electric contacts
Integrated circuits
Semiconductor device fabrication
(process for forming cobalt and cobalt silicide materials in copper contact applications)

IT 7440-48-4, Cobalt, properties 11104-62-4, Cobalt silicide
RL: PRP (Properties); TEM (Technical or engineered material use); USES (Uses)
(process for forming cobalt and cobalt silicide materials in copper contact applications)

IT 1277-43-6, Bis(cyclopentadienyl)cobalt 1590-87-0, Disilane 7803-62-5, Silane, reactions 10210-68-1, Dicobalt octa(carbonyl) 12078-25-0, Cyclopentadienyl cobalt dicarbonyl 12129-77-0, Pentamethylcyclopentadienyl cobalt dicarbonyl 12144-85-3, Tricarbonyl allyl cobalt 12146-91-7, Bis(methylcyclopentadienyl)cobalt 12306-95-5 14096-82-3, Nitrosyl cobalt tricarbonyl 32876-13-4 73231-01-3 75297-02-8 80848-36-8 154033-77-9 163451-74-9
RL: RCT (Reactant); RACT (Reactant or reagent)
(process for forming cobalt and cobalt silicide materials in copper contact applications)

IT 7440-21-3, Silicon, uses
RL: TEM (Technical or engineered material use); USES (Uses)
(process for forming cobalt and cobalt silicide

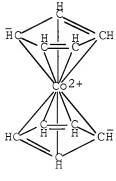
materials in copper contact applications)
IT 7440-48-4, Cobalt, properties 11104-62-4, Cobalt silicide
RL: PRP (Properties); TEM (Technical or engineered material use); USES (Uses)
(process for forming cobalt and cobalt silicide materials in copper contact applications)
RN 7440-48-4 HCAPLUS
CN Cobalt (CA INDEX NAME)

Co

RN 11104-62-4 HCAPLUS
CN Cobalt silicide (CA INDEX NAME)

Component	Ratio	Component Registry Number
Co	x	7440-48-4
Si	x	7440-21-3

IT 1277-43-6, Bis(cyclopentadienyl)cobalt 1590-87-0, Disilane 7803-62-5, Silane, reactions 10210-68-1, Dicobalt octa(carbonyl) 12078-25-0, Cyclopentadienyl cobalt dicarbonyl 12129-77-0, Pentamethylcyclopentadienyl cobalt dicarbonyl 12144-85-3, Tricarbonyl allyl cobalt 12146-91-7, Bis(methylcyclopentadienyl)cobalt 12306-95-5 32876-13-4 73231-01-3 75297-02-8 80848-36-8 154033-77-9 163451-74-9
RL: RCT (Reactant); RACT (Reactant or reagent)
(process for forming cobalt and cobalt silicide materials in copper contact applications)
RN 1277-43-6 HCAPLUS
CN Cobaltocene (CA INDEX NAME)



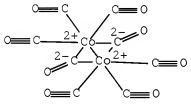
RN 1590-87-0 HCAPLUS
CN Disilane (CA INDEX NAME)

H3Si—SiH3

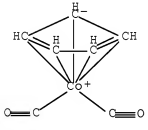
RN 7803-62-5 HCAPLUS
CN Silane (CA INDEX NAME)

SiH4

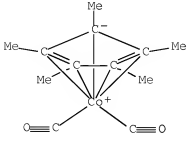
RN 10210-68-1 HCAPLUS
CN Cobalt, di-μ-carbonylhexacarbonyldi-, (Co-Co) (CA INDEX NAME)



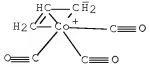
RN 12078-25-0 HCAPLUS
CN Cobalt, dicarbonyl(η5-2,4-cyclopentadien-1-yl)- (CA INDEX NAME)



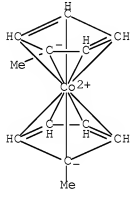
RN 12129-77-0 HCAPLUS
CN Cobalt, dicarbonyl[(1,2,3,4,5-η)-1,2,3,4,5-pentamethyl-2,4-cyclopentadien-1-yl]- (CA INDEX NAME)



RN 12144-85-3 HCAPLUS
CN Cobalt, tricarbonyl(η3-2-propenyl)- (CA INDEX NAME)

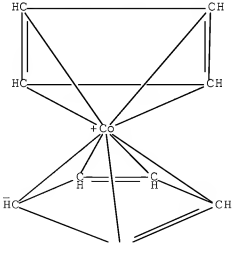


RN 12146-91-7 HCAPLUS
CN Cobaltocene, 1,1'-dimethyl- (9CI) (CA INDEX NAME)



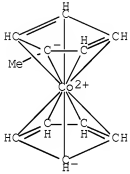
RN 12306-95-5 HCAPLUS
CN Cobalt, (η4-1,3-cyclobutadiene)(η5-2,4-cyclopentadien-1-yl)- (CA INDEX NAME)

PAGE 1-A

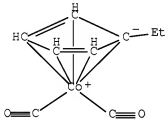


PAGE 2-A

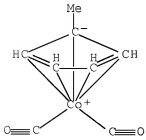
RN 32876-13-4 HCAPLUS
CN Cobaltocene, methyl- (9CI) (CA INDEX NAME)



RN 73231-01-3 HCAPLUS
CN Cobalt, dicarbonyl[(1,2,3,4,5-η)-1-ethyl-2,4-cyclopentadien-1-yl]-
(9CI) (CA INDEX NAME)

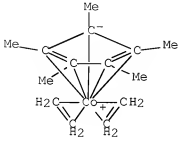


RN 75297-02-8 HCAPLUS
CN Cobalt, dicarbonyl[(1,2,3,4,5-η)-1-methyl-2,4-cyclopentadien-1-yl]-
(CA INDEX NAME)



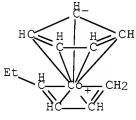
RN 80848-36-8 HCAPLUS

CN Cobalt, bis(η2-ethene)[(1,2,3,4,5-η)-1,2,3,4,5-pentamethyl-2,4-cyclopentadien-1-yl]- (9CI) (CA INDEX NAME)



RN 154033-77-9 HCAPLUS

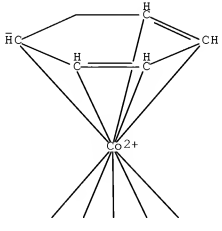
CN Cobalt, (η5-2,4-cyclopentadien-1-yl)[(1,2,3,4-η)-1,3-hexadiene]-, (E)- (9CI) (CA INDEX NAME)



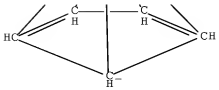
RN 163451-74-9 HCAPLUS

CN Cobalt, [(1,2,3,4,5-η)-2,4-cyclohexadien-1-yl](η5-2,4-cyclopentadien-1-yl)- (CA INDEX NAME)

PAGE 1-A



PAGE 2-A



L95 ANSWER 2 OF 28 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 2007:1324969 HCAPLUS Full-text
DN 147:552396
TI Semiconductor memory with data retention liner
IN Ngo, Minh Van; Halliyal, Arvind; Kamal, Tazrien; Shiraiwa, Hidehiko; Sugino, Rinji; Hopper, Dawn; Gao, Pei-Yuan
PA Spansion LLC, USA
SO U.S., 12pp., Cont.-in-part of U.S. Ser. No 109,527. Abandoned
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

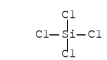
PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 7297592	B1	20071120	US 2005-195201	20050801 <--
PRAI US 2002-109527	B2	20020327	<--	

AB A manufacturing method for a dual bit flash memory includes providing a semiconductor substrate and depositing a charge-trapping dielec. layer with the depositing performed without using NH3 at an ultra-slow deposition rate. First and 2nd bitlines are implanted and a wordline layer is deposited. A hard mask layer is deposited over the wordline layer. A photoresist is deposited over the wordline layer and used to form a hard mask. The photoresist is removed. The wordline layer is processed using the hard mask to form a wordline and the hard mask is removed. A reduced H, high-d. data retention liner to reduce charge loss, covers the wordline and the charge-trapping dielec. layer. An interlayer dielec. layer is deposited over the data retention liner.
INCL 438257000; 257-E21.179
CC 76-3 (Electric Phenomena)
IT Integrated circuits
(in semiconductor memory with data retention liner)
IT Dielectric films
Ion implantation
Photoresists
Semiconductor memory devices
(semiconductor memory with data retention liner)
IT 11104-62-4, Cobalt silicide 12738-91-9, Titanium silicide 39467-10-2, Nickel silicide
RL: TEM (Technical or engineered material use); USES (Uses)
(contacts in semiconductor memory with data retention liner)
IT 10026-04-7, Tetrachlorosilane
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(in semiconductor memory with data retention liner)

IT 11104-62-4, Cobalt silicide
RL: TEM (Technical or engineered material use); USES (Uses)
(contacts in semiconductor memory with data retention liner)
RN 11104-62-4 HCAPLUS
CN Cobalt silicide (CA INDEX NAME)

Component	Ratio	Component Registry Number
Co	x	7440-48-4
Si	x	7440-21-3

IT 10026-04-7, Tetrachlorosilane
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(in semiconductor memory with data retention liner)
RN 10026-04-7 HCAPLUS
CN Silane, tetrachloro- (CA INDEX NAME)



RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L95 ANSWER 3 OF 28 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 2005:348939 HCAPLUS Full-text
DN 142:421524
TI Heterogeneous activation layers formed by ionic and electroless reactions used for IC interconnect capping layers
IN Lopatin, Sergey D.; Shanmugasundram, Arulkumar; Shacham-diamand, Yosef; Weidman, Timothy; Lubomirsky, Dmitry
PA Applied Materials, Inc., USA
SO U.S. Pat. Appl. Publ., 19 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 20050085031	A1	20050421	US 2004-967099	20041015 <--
PRAI US 2003-511993P	P	20031015 <--		

AB There is a need for a method and composition to form an electroless layer, such as a capping layer with strong adhesion to a conductive layer, low elec. resistance and strong barrier properties. Embodiments of the invention generally provide compns. of activation-alloy solns., methods to deposit activation-alloys and electronic devices including activation-alloys and capping layers. In one embodiment, a method for depositing a capping layer for a semiconductor device is provided which includes exposing a conductive layer on a substrate surface to an activation-alloy solution, forming an activation-alloy layer on the conductive layer using the activation-alloy solution, and depositing the capping layer on the activation-alloy layer using an electroless deposition solution
IC ICM H01L0021-8238
INCL 438222000

CC 76-2 (Electric Phenomena)
Section cross-reference(s): 48, 56
IT Films
(elec. conductive; heterogeneous alloy activation layers formed by ionic and electroless reactions used for IC interconnect capping layers)
IT Coating process
(electroless; heterogeneous alloy activation layers formed by ionic and electroless reactions used for IC interconnect capping layers)
IT Electric conductors
(films; heterogeneous alloy activation layers formed by ionic and electroless reactions used for IC interconnect capping layers)
IT Integrated circuits
Interconnections, electric
Ion implantation
Semiconductor device fabrication
Surfactants
(heterogeneous alloy activation layers formed by ionic and electroless reactions used for IC interconnect capping layers)
IT 60-00-4, EDTA, processes 71-48-7, Cobalt acetate 71-50-1, Acetate, processes 77-92-9, Citric acid, processes 87-69-4, Tartaric acid, processes 97-94-9, Triethylborane 107-15-3, Ethylenediamine, processes 126-44-3, Citrate, processes 142-71-2, Copper acetate 298-12-4, Glyoxylic acid 302-01-2, Hydrazine, processes 992-94-9, Methylsilane 1111-74-6, Dimethylsilane 1333-74-0, Hydrogen, processes 1336-21-6, Ammonium hydroxide ((NH4)(OH)) 1344-67-8, Copper chloride 1590-87-0, Disilane 2814-79-1, Ethylsilane 3375-31-3, Palladium diacetate 4109-96-0, Dichlorosilane 6303-21-5, Hypophosphorous acid 7646-79-9, Cobalt chloride (CoCl2), processes 7647-01-0, Hydrochloric acid, processes 7647-10-1, Palladium chloride 7664-39-3, Hydrofluoric acid, processes 7664-41-7, Ammonia, processes 7664-93-9, Sulfuric acid, processes 7681-65-4, Copper iodide (CuI) 7758-89-6, Copper chloride (CuCl) 7758-98-7, Copper sulfate (CuSO4), processes 7782-44-7, Oxygen, processes 7783-03-1, Tungstic acid 7783-26-8, Trisilane 7783-29-1, Tetrasilane 7787-70-4, Copper bromide (CuBr) 7790-75-2, Calcium tungstate 7803-62-5, Silane, processes 10024-97-2, Nitrous oxide, processes 10102-43-9, Nitric oxide, processes 10102-44-0, Nitrogen dioxide, processes 10124-43-3, Cobalt sulfate (CoSO4) 12261-30-2 13283-31-3, Borane, processes 13394-86-0, DMAB 13395-16-9 13465-77-5, Hexachlorodisilane 13566-03-5, Palladium sulfate 14024-48-7 14024-61-4, Palladium acetylacetonate 14040-05-2 14220-26-9, Copper acetylacetonate 14781-45-4 15214-66-1 15855-70-6 19287-45-7, Diborane 19624-22-7, Pentaborane 32992-96-4 33292-37-4 36350-66-0, Triborane(9) 51811-79-1, RE 610 53199-31-8 60349-62-4, Tetraborane(12) 64916-48-9 85908-78-7 86233-74-1 137007-13-7 139566-53-3 152219-08-4 220409-27-8 308847-89-4 666854-30-4 850252-13-0 850252-14-1 850252-15-2
RL: CPS (Chemical process); NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(heterogeneous alloy activation layers formed by ionic and electroless reactions used for IC interconnect capping layers)
IT 7440-50-8P, Copper, processes 12618-78-9P 12647-46-0P 39286-82-3P 329717-28-4P, Cobalt 10, copper 100 (atomic) 850252-12-9P, Copper 10, palladium 150 (atomic)
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PYP (Physical process); SPN (Synthetic preparation); PREP (Preparation); PROC (Process); USES (Uses)
(heterogeneous alloy activation layers formed by ionic and electroless reactions used for IC interconnect capping layers)

IT 1590-87-0, Disilane 4109-96-0, Dichlorosilane
7783-26-8, Trisilane 7783-29-1, Tetrasilane
7803-62-5, Silane, processes 13465-77-5,
Hexachlorodisilane 14024-48-7
RL: CPS (Chemical process); NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(heterogeneous alloy activation layers formed by ionic and electroless reactions used for IC interconnect capping layers)

RN 1590-87-0 HCAPLUS
CN Disilane (CA INDEX NAME)

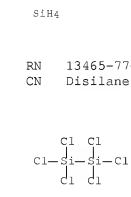
RN 4109-96-0 HCAPLUS
CN Silane, dichloro- (CA INDEX NAME)

RN 7783-26-8 HCAPLUS
CN Trisilane (CA INDEX NAME)

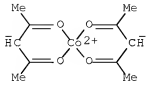
RN 7783-29-1 HCAPLUS
CN Tetrasilane (6CI, 7CI, 8CI, 9CI) (CA INDEX NAME)

RN 7803-62-5 HCAPLUS
CN Silane (CA INDEX NAME)

RN 13465-77-5 HCAPLUS
CN Disilane, 1,1,1,2,2,2-hexachloro- (CA INDEX NAME)



RN 14024-48-7 HCAPLUS
CN Cobalt, bis(2,4-pentanedionato-κO2,κO4)-, (SP-4-1)- (CA INDEX NAME)



L95 ANSWER 4 OF 28 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 2004:1060710 HCAPLUS Full-text
DN 142:47314
TI Method of fabricating a high performance MOSFET device featuring formation of an elevated source/drain region
IN Wang, Yin-Pin; Chang, Chih-Sheng
PA Taiwan Semiconductor Manufacturing Co., Ltd., Taiwan
SO U.S. Pat. Appl. Publ., 9 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 20040248369	A1	20041209	US 2003-455038	20030605 <--
	US 6902980	B2	20050607		
	US 20050095799	A1	20050505	US 2004-971624	20041022 <--
	US 7129547	B2	20061031		
PRAI	US 2003-455038	A3	20030605	<--	

AB A method of fabricating a MOSFET device featuring a raised source/drain structure on a heavily doped source/drain region as well as on a portion of a lightly doped source/drain (LDD) region, after removal of an insulator spacer component, has been developed. After formation of an LDD region a composite insulator spacer, comprised of an underlying silicon oxide spacer component and an overlying silicon nitride spacer component, is formed on the sides of a gate structure. Formation of a heavily doped source/drain is followed by removal of the silicon nitride spacer resulting in recessing of, and damage formation to, the heavily doped source/drain region, as well as recessing of the gate structure. Removal of a horizontal component of the silicon oxide spacer component results in addnl. recessing of the heavily doped source/drain region, and of the gate structure. A selective epitaxial growth procedure is then used to form a raised, single crystalline silicon structure on the recessed and damaged heavily doped source/drain and LDD regions, while a polycryst. silicon structure is grown on the underlying recessed gate structure. The metal silicide is then formed on the raised, single crystalline silicon structure and on the polycryst. silicon structure.
IC ICM H01L0021-336
INCL 438305000
CC 76-3 (Electric Phenomena)
IT Films
(elec. conductive; removal of insulator spacer and selective epitaxial growth in fabrication of high-performance MOSFET with elevated source/drain region)
IT Electric conductors

(films; removal of insulator spacer and selective epitaxial growth in fabrication of high-performance MOSFET with elevated source/drain region)
IT Gate contacts
MOSFET (transistors)
(removal of insulator spacer and selective epitaxial growth in fabrication of high-performance MOSFET with elevated source/drain region)
IT 1590-87-0, Disilane 7803-62-5, Silane, reactions
RL: RCT (Reactant); RACT (Reactant or reagent)
(precursor; removal of insulator spacer and selective epitaxial growth in fabrication of high-performance MOSFET with elevated source/drain region)
IT 11104-62-4, Cobalt silicide 12627-41-7, Tungsten silicide 12738-91-9, Titanium silicide 37189-51-8, Zirconium silicide 39467-10-2, Nickel silicide 52953-72-7, Tantalum silicide
RL: DEV (Device component use); USES (Uses)
(removal of insulator spacer and selective epitaxial growth in fabrication of high-performance MOSFET with elevated source/drain region)
IT 1590-87-0, Disilane 7803-62-5, Silane, reactions
RL: RCT (Reactant); RACT (Reactant or reagent)
(precursor; removal of insulator spacer and selective epitaxial growth in fabrication of high-performance MOSFET with elevated source/drain region)
RN 1590-87-0 HCAPLUS
CN Disilane (CA INDEX NAME)

RN 7803-62-5 HCAPLUS
CN Silane (CA INDEX NAME)

IT 11104-62-4, Cobalt silicide
RL: DEV (Device component use); USES (Uses)
(removal of insulator spacer and selective epitaxial growth in fabrication of high-performance MOSFET with elevated source/drain region)
RN 11104-62-4 HCAPLUS
CN Cobalt silicide (CA INDEX NAME)

Component	Ratio	Component Registry Number
Co	x	7440-48-4
Si	x	7440-21-3

RE.CNT 18 THERE ARE 18 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L95 ANSWER 5 OF 28 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 2004:1045667 HCAPLUS Full-text

DN 142:289312
TI Method for forming the semiconductor element with recessed source/drain junction
IN Zhang, Guohua; Huang, Wenxin
PA Macronix International Co., Ltd., Peop. Rep. China
SO Faming Zhuanli Shenqing Gongkai Shuomingshu, 21 pp.
CODEN: CNXXEV
DT Patent
LA Chinese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI CN 1471139	A	20040128	CN 2002-140775	20020724 <--
CN 1242457	C	20060215		
PRAI CN 2002-140775		20020724 <--		

AB The method comprises forming a gate structure that has a top cover layer on a substrate, forming a spacer on the sidewall of the gate structure, etching with the spacer and the top cover layer to form an opening in the substrate beside of each sidewall, depositing the selective Si1-xGex thin film in the opening via rapid thermal CVD from Si2H6-GeH4-B2H6 or SiH2C12-GeH4-B2H6 at 500° and 1-20 torr to form a source/drain with a shallow junction, and then forming a metal silicide (CoSix or NiSix) layer on the source/drain.

IC ICM H01L0021-285
ICS H01L0021-336
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 74
ST semiconductor element recessed source drain junction silicon germanium; silane germane borane cobalt nickel silicide gate etching semiconductor
IT Etching
Films
Gate contacts
Semiconductor device fabrication
Semiconductor devices
Semiconductor junctions
(method for making semiconductor element with recessed source/drain junction)
IT 78-10-4, Tetraethoxysilane 1590-87-0, Disilane 2551-62-4, Sulfur hexafluoride 4109-96-0, Dichlorosilane 7782-65-2, Germane 19287-45-7, Diborane
RL: RCT (Reactant); RACT (Reactant or reagent)
(method for making semiconductor element with recessed source/drain junction)
IT 11104-62-4, Cobalt silicide 39467-10-2, Nickel silicide
RL: TEM (Technical or engineered material use); USES (Uses)
(method for making semiconductor element with recessed source/drain junction)
IT 1590-87-0, Disilane 4109-96-0, Dichlorosilane
RL: RCT (Reactant); RACT (Reactant or reagent)
(method for making semiconductor element with recessed source/drain junction)
RN 1590-87-0 HCAPLUS
CN Disilane (CA INDEX NAME)

RN 4109-96-0 HCAPLUS
CN Silane, dichloro- (CA INDEX NAME)

IT 11104-62-4, Cobalt silicide
RL: TEM (Technical or engineered material use); USES (Uses)
(method for making semiconductor element with recessed source/drain junction)
RN 11104-62-4 HCAPLUS
CN Cobalt silicide (CA INDEX NAME)

Component	Ratio	Component Registry Number
Co	x	7440-48-4
Si	x	7440-21-3

L95 ANSWER 6 OF 28 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 2004:312308 HCAPLUS Full-text
DN 140:348917
TI Method of integrating L-shaped spacers in a high performance CMOS process via use of an oxide-nitride-doped oxide spacer
IN Quek, Elgin
PA Chartered Semiconductor Manufacturing Ltd., Singapore
SO U.S. Pat. Appl. Publ., 10 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 20040072435	A1	20040415	US 2002-267206	20021009 <--
US 6815355	B2	20041109		
SG 111158	A1	20050530	SG 2003-5908	20031007 <--
PRAI US 2002-267206	A	20021009 <--		

AB A process for fabricating a complementary metal oxide semiconductor (CMOS), device featuring composite insulator spacer shapes which allow P channel (PMOS), short channel effects to be minimized, and allow redns. in resistance for N channel (NMOS), source/drain extension regions to be realized, was developed. The process features initial composite insulator spacers formed in the sides of gate structures after definition of the NMOS and PMOS source/drain extension regions. The initial composite insulator spacer, comprised of an underlying Si oxide component, an L-shaped Si nitride component, and an overlying doped oxide component, is then used for definition of the PMOS heavily doped source/drain region, allowing for adequate space between the heavily doped source/drain and channel regions, thus reducing the risk of short channel effects. After removal of the doped oxide component, the L-shaped composite insulator spacer was used to define, via ion implantation procedures, an NMOS heavily doped region, featuring a portion of the heavily doped source/drain region formed underlying a horizontal feature of the L-shaped Si nitride component, therefore compensating a portion of the NMOS source/drain extension region, and resulting in the desired reduction in source/drain resistance.
IC ICM H01L0021-302
ICS H01L0021-461; H01L0021-311

INCL 438691000
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 48
IT MOS devices
(complementary; method of integrating L-shaped spacers in high performance CMOS process via use of oxide-nitride-doped oxide spacer)
IT Dielectric films
Dopants
Doping
Gate contacts
Ion implantation
Semiconductor device fabrication
(method of integrating L-shaped spacers in high performance CMOS process via use of oxide-nitride-doped oxide spacer)
IT 75-46-7, Trifluoromethane 75-73-0, Carbon fluoride (CF4) 78-10-4, TEOS 7664-39-3, Hydrogen fluoride, processes 7782-50-5, Chlorine, processes 7784-42-1, Arsine 7803-51-2, Phosphine 7803-62-5, Silane, processes
RL: CPS (Chemical process); NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(method of integrating L-shaped spacers in high performance CMOS process via use of oxide-nitride-doped oxide spacer)
IT 7631-86-9, Silica, processes 11104-62-4, Cobalt silicide 12033-89-5, Silicon nitride, processes 12738-91-9, Titanium silicide 39467-10-2, Nickel silicide
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process)
(method of integrating L-shaped spacers in high performance CMOS process via use of oxide-nitride-doped oxide spacer)
IT 7803-62-5, Silane, processes
RL: CPS (Chemical process); NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(method of integrating L-shaped spacers in high performance CMOS process via use of oxide-nitride-doped oxide spacer)
RN 7803-62-5 HCAPLUS
CN Silane (CA INDEX NAME)

SiH4

IT 11104-62-4, Cobalt silicide
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process)
(method of integrating L-shaped spacers in high performance CMOS process via use of oxide-nitride-doped oxide spacer)
RN 11104-62-4 HCAPLUS
CN Cobalt silicide (CA INDEX NAME)

Component	Ratio	Component Registry Number
Co	x	7440-48-4
Si	x	7440-21-3

RE.CNT 12 THERE ARE 12 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L95 ANSWER 7 OF 28 HCAPLUS COPYRIGHT 2009 ACS on STN

AN 2004:219978 HCAPLUS Full-text
DN 140:262596
TI Method for forming quantum dot
IN Park, Sung-eon
PA Hynix Semiconductor Inc., S. Korea
SO U.S. Pat. Appl. Publ., 11 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 20040053469	A1	20040318	US 2002-320402	20021217 <--
	US 6730531	B2	20040504		
	TW 251879	B	20060321	TW 2002-91136873	20021220 <--
	CN 1484277	A	20040324	CN 2003-122555	20030418 <--
PRAI	KR 2002-56462	A	20020917 <--		

AB The present invention relates to a method for forming a plurality of quantum dots providing simultaneously reliability and mass production effects. The present invention includes the steps of: a method for forming a quantum dot, including the steps of: forming a 1st insulating layer on a semiconductor substrate; forming an opening that exposes the semiconductor substrate by etching the 1st insulating layer; forming a single crystal semiconductor layer in the opening and on the 1st insulating layer adjacent to the opening; and forming a quantum dot on the 1st insulating layer adjacent to the opening by removing the single crystal semiconductor layer in the opening and portions of the singly crystal layer on the 1st insulating layer adjacent to the opening.

IC ICM H01L0021-00
ICS H01L0021-336; H01L0021-8234
INCL 438264000; 438962000
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 48
IT Films
(elec. conductive; in fabrication of quantum dots)
IT Semiconductor films
(epitaxial; in fabrication of quantum dots)
IT MOSFET (transistors)
Quantum dot devices
Semiconductor device fabrication
(fabrication of quantum dots)
IT Electric conductors
(films; in fabrication of quantum dots)
IT Contact holes
Dielectric films
Etching
Etching masks
(in fabrication of quantum dots)
IT Epitaxial films
(semiconductive; in fabrication of quantum dots)
IT Transistors
(single electron; fabrication of quantum dots)
IT 1333-74-0, Hydrogen, processes 4109-96-0, Silicon chloride hydride (SiCl2H2) 7647-01-0, Hydrogen chloride, processes 7803-51-2, Phosphine (PH3) 7803-62-5, Silicon hydride (SiH4), processes
RL: CPS (Chemical process); NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in fabrication of quantum dots)
IT 7440-21-3, Silicon, processes 7631-86-9, Silicon dioxide, processes 11104-62-4, Cobalt silicide 11148-21-3 12033-89-5, Silicon nitride, processes

RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(in fabrication of quantum dots)

IT 4109-96-0, Silicon chloride hydride (SiC12H2) 7803-62-5, Silicon hydride (SiH4), processes
RL: CPS (Chemical process); NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in fabrication of quantum dots)

RN 4109-96-0 HCAPLUS
CN Silane, dichloro- (CA INDEX NAME)

RN 7803-62-5 HCAPLUS
CN Silane (CA INDEX NAME)

IT 11104-62-4, Cobalt silicide
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(in fabrication of quantum dots)

RN 11104-62-4 HCAPLUS
CN Cobalt silicide (CA INDEX NAME)

Component	Ratio	Component Registry Number
Co	x	7440-48-4
Si	x	7440-21-3

RE.CNT 9 THERE ARE 9 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L95 ANSWER 8 OF 28 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 2004:3600 HCAPLUS Full-text
DN 140:69057
TI Fabrication of a raised source/drain of a semiconductor device
IN Chang, Kent Kuohua
PA Macronix International Co., Ltd., Taiwan
SO U.S. Pat. Appl. Publ., 11 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 20040002194	A1	20040101	US 2002-64561	20020726 <--
	US 6737324	B2	20040518		
	TW 284348	B	20070721	TW 2002-91114489	20020701 <--
	CN 1469435	A	20040121	CN 2002-126347	20020718 <--
PRAI	TW 2002-91114489	A	20020701	<--	

AB The invention relates to the fabrication of a raised source/drain of a semiconductor device, where the raised structure lowers resistance and

prevents the short channel effect and junction leakage. The fabrication process consists of the steps of (i) forming a gate structure on the substrate; (ii) forming a source/drain with a shallow junction in the substrate beside the gate structure; (iii) forming a spacer on sidewalls of the gate structure; and (iv) forming an elevated SiGe layer on the gate structure and the source/drain with a shallow junction, where the elevated layer formed on the source/drain serves as an elevated source/drain layer.

IC ICM H01L0021-336
INCL 438300000
CC 76-3 (Electric Phenomena)
IT Silicides
RL: DEV (Device component use); USES (Uses)
(SiGe raised feature coated by; fabrication of raised source/drain of semiconductor device)
IT 11104-62-4, Cobalt silicide 39467-10-2, Nickel silicide
RL: DEV (Device component use); USES (Uses)
(SiGe raised feature coated by; fabrication of raised source/drain of semiconductor device)
IT 1590-87-0, Disilane 4109-96-0, Dichlorosilane 7782-65-2, Germane
RL: RCT (Reactant); RACT (Reactant or reagent)
(vapor deposition precursor; fabrication of raised source/drain of semiconductor device)
IT 11104-62-4, Cobalt silicide
RL: DEV (Device component use); USES (Uses)
(SiGe raised feature coated by; fabrication of raised source/drain of semiconductor device)
RN 11104-62-4 HCAPLUS
CN Cobalt silicide (CA INDEX NAME)

Component	Ratio	Component Registry Number
Co	x	7440-48-4
Si	x	7440-21-3

IT 1590-87-0, Disilane 4109-96-0, Dichlorosilane
RL: RCT (Reactant); RACT (Reactant or reagent)
(vapor deposition precursor; fabrication of raised source/drain of semiconductor device)
RN 1590-87-0 HCAPLUS
CN Disilane (CA INDEX NAME)

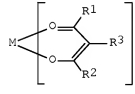
RN 4109-96-0 HCAPLUS
CN Silane, dichloro- (CA INDEX NAME)

L95 ANSWER 9 OF 28 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 2003:902526 HCAPLUS Full-text

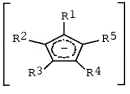
DN 139:373109
TI Material for deposition of silicide film, method for deposition of silicide film, and MOSFET
IN Machida, Hideaki; Oshita, Akio; Ishikawa, Masato; Kada, Takeshi
PA Tri Chemical Laboratory Inc., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2003328130	A	20031119	JP 2002-141007	20020516 <--
KR 2006080907	A	20060711	KR 2006-50517	20060605 <--
PRAI JP 2002-141007	A	20020516	<--	
KR 2003-22556	A3	20030410	<--	

OS MARPAT 139:373109
GI



I



II

AB A source material for CVD of a Co and/or Ni silicide film comprises (I), where M = Co or Ni, n = 2 or 3, and R1-3 = alkyl, or (II), where M = Co or Ni, and R1-5 = alkyl or H. The material is useful for CVD of a silicide conductive film of a MOSFET.
IC ICM C23C0016-18
ICS C01B0033-06; C07C0049-92; C07F0007-08; C07F0015-04; C07F0015-06; C07F0017-00; C23C0016-42
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 75
ST nickel cobalt silicide film conductor CVD source material MOSFET
IT Vapor deposition process
(chemical; source material for deposition of silicide film, method for deposition of silicide conductor film, and MOSFET)
IT Films
(elec. conductive; source material for deposition of silicide film, method for deposition of silicide conductor film, and MOSFET)
IT Electric conductors
(films; source material for deposition of silicide film, method for deposition of silicide conductor film, and MOSFET)
IT MOSFET (transistors)
(source material for deposition of silicide film, method for deposition of silicide conductor film, and MOSFET)
IT 12017-12-8, Cobalt disilicide 39467-10-2, Nickel silicide 140418-11-7, Cobalt nickel silicide

RL: CPS (Chemical process); DEV (Device component use); PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(source material for deposition of silicide film, method for deposition of silicide conductor film, and MOSFET)

IT 60-34-4, Methylhydrazine 64-17-5, Ethanol, uses 75-07-0, Ethylaldehyde, uses 75-50-3, uses 542-91-6, Diethylsilane 617-86-7, Triethylsilane 993-07-7, Trimethylsilane 1111-74-6, Dimethylsilane 1293-95-4, 1,1'-Dimethylnickelocene 1333-74-0, Hydrogen, uses 1590-87-0, Disilane 3264-82-2 6117-91-5, 2-Buten-1-ol 7732-18-5, Water, uses 7783-26-8, Trisilane 7803-62-5, Silane, uses 12146-91-7, 1,1'-Dimethylcobaltocene 13986-53-3, Bis(2,2,6,6-tetramethyl-3,5-heptanedionato) cobalt 14024-48-7, Cobalt diacetylacetonate 14481-08-4, Bis(2,2,6,6-tetramethyl-3,5-heptanedionato)nickel 14877-41-9, Tris(2,2,6,6-tetramethyl-3,5-heptanedionato) cobalt 21679-46-9, Tris(2,4-pentanedionato) cobalt 31886-51-8, 1,1'-Diethylnickelocene 55940-05-1, 1,1'-Diethylcobaltocene 57197-55-4, 1,1'-Diisopropylnickelocene 60064-86-0, 1,1'-Dibutylcobaltocene 60064-87-1, 1,1'-Dibutylnickelocene 61993-73-5, 1,1'-Diisopropylcobaltocene
RL: NUU (Other use, unclassified); USES (Uses)
(source material for deposition of silicide film, method for deposition of silicide conductor film, and MOSFET)

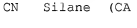
IT 12017-12-8, Cobalt disilicide
RL: CPS (Chemical process); DEV (Device component use); PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(source material for deposition of silicide film, method for deposition of silicide conductor film, and MOSFET)

RN 12017-12-8 HCAPLUS
CN Cobalt silicide (CoSi2) (CA INDEX NAME)

IT 1590-87-0, Disilane 7783-26-8, Trisilane 7803-62-5, Silane, uses 12146-91-7, 1,1'-Dimethylcobaltocene 13986-53-3, Bis(2,2,6,6-tetramethyl-3,5-heptanedionato)cobalt 14024-48-7, Cobalt diacetylacetonate 14877-41-9, Tris(2,2,6,6-tetramethyl-3,5-heptanedionato)cobalt 21679-46-9, Tris(2,4-pentanedionato)cobalt 55940-05-1, 1,1'-Diethylcobaltocene 60064-86-0, 1,1'-Dibutylcobaltocene 61993-73-5, 1,1'-Diisopropylcobaltocene
RL: NUU (Other use, unclassified); USES (Uses)
(source material for deposition of silicide film, method for deposition of silicide conductor film, and MOSFET)

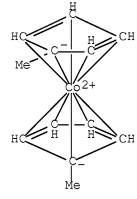
RN 1590-87-0 HCAPLUS
CN Disilane (CA INDEX NAME)

RN 7783-26-8 HCAPLUS
CN Trisilane (CA INDEX NAME)

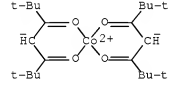


RN 7803-62-5 HCAPLUS
CN Silane (CA INDEX NAME)

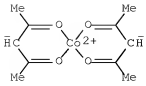
RN 12146-91-7 HCAPLUS
CN Cobaltocene, 1,1'-dimethyl- (9CI) (CA INDEX NAME)



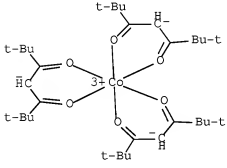
RN 13986-53-3 HCAPLUS
CN Cobalt, bis(2,2,6,6-tetramethyl-3,5-heptanedionato-κO3,κO5)-, (T-4)- (CA INDEX NAME)



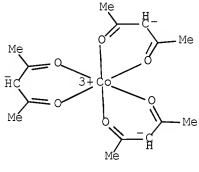
RN 14024-48-7 HCAPLUS
CN Cobalt, bis(2,4-pentanedionato-κO2,κO4)-, (SP-4-1)- (CA INDEX NAME)



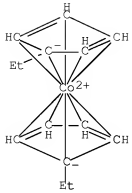
RN 14877-41-9 HCAPLUS
CN Cobalt, tris(2,2,6,6-tetramethyl-3,5-heptanedionato-κO3,κO5)-, (OC-6-11)- (CA INDEX NAME)



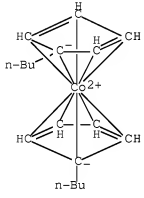
RN 21679-46-9 HCAPLUS
CN Cobalt, tris(2,4-pentanedionato-κO2,κO4)-, (OC-6-11)- (CA INDEX NAME)



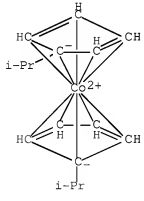
RN 55940-05-1 HCAPLUS
CN Cobaltocene, 1,1'-diethyl- (CA INDEX NAME)



RN 60064-86-0 HCAPLUS
CN Cobaltocene, 1,1'-dibutyl- (CA INDEX NAME)



RN 61993-73-5 HCAPLUS
CN Cobaltocene, 1,1'-bis(1-methylethyl)- (CA INDEX NAME)



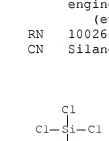
L95 ANSWER 10 OF 28 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 2002:143138 HCAPLUS Full-text
DN 136:192632
TI Fabrication of a conductive spacer in a via with improved adhesion

IN Gonzalez, Fernando; Blalock, Guy
PA Micron Technology, Inc., USA
SO U.S. Pat. Appl. Publ., 10 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 20020020835	A1	20020221	US 1996-595806	19960202 <--
	US 6420786	B2	20020716		
	US 6171964	B1	20010109	US 1998-13633	19980126 <--
	US 6222273	B1	20010424	US 1998-16753	19980130 <--
PRAI	US 1996-595806	A3	19960202	<--	

AB A method of constructing a conductive via spacer within a dielec. layer located between a 1st metal layer and a 2nd metal layer includes the steps of depositing a conductive spacer layer within the opening and over the 1st metal layer. A portion of the conductive spacer layer is removed to leave a conductive spacer within the opening. The 2nd metal layer is deposited over the spacer to complete the connection between the 1st and 2nd metal layers. The spacer preferably comprises a material selected from the group comprising refractory metal silicides and nitrides. The spacer is preferably tapered and the via may include a glue layer to improve the adherence of the spacer to the dielec. layer.

IC ICM H01L0047-00
INCL 257001000
CC 76-2 (Electric Phenomena)
IT Integrated circuits
(method of forming a conductive spacer in a via)
IT Dielectric films
(method of forming a conductive spacer in a via using)
IT 56-23-5, Tetrachloromethane, processes 7647-01-0, Hydrogen chloride, processes 7782-50-5, Chlorine, processes 10026-04-7, Tetrachlorosilane 10294-34-5, Trichloroborane
RL: CPS (Chemical process); NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(etchant; method of forming a conductive spacer in a via)
IT 11104-62-4, Cobalt silicide 12738-91-9, Titanium silicide
RL: CPS (Chemical process); DEV (Device component use); PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(method of forming a conductive spacer in a via)
IT 10026-04-7, Tetrachlorosilane
RL: CPS (Chemical process); NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(etchant; method of forming a conductive spacer in a via)
RN 10026-04-7 HCAPLUS
CN Silane, tetrachloro- (CA INDEX NAME)



IT 11104-62-4, Cobalt silicide
RL: CPS (Chemical process); DEV (Device component use); PEP (Physical,

engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(method of forming a conductive spacer in a via)
RN 11104-62-4 HCAPLUS
CN Cobalt silicide (CA INDEX NAME)

Component	Ratio	Component Registry Number
Co	x	7440-48-4
Si	x	7440-21-3

L95 ANSWER 11 OF 28 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 2002:143061 HCAPLUS Full-text
DN 136:192759
TI Method of fabrication of multi-gate semiconductor device with vertical channel current
IN Cleeves, James M.; Subramanian, Vivek
PA Matrix Semiconductor, Inc., USA
SO PCT Int. Appl., 37 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI WO 2002015278	A2	20020221	WO 2001-US41674	20010813 <--
WO 2002015278	A3	20020613		
W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW				
RW: GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW, AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR, BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG				
US 6580124	B1	20030617	US 2000-639577	20000814 <--
AU 2001091257	A	20020225	AU 2001-91257	20010813 <--
TW 505998	B	20021011	TW 2001-90119948	20010813 <--
US 20030139011	A1	20030724	US 2002-254878	20020926 <--
US 6677204	B2	20040113		
PRAI US 2000-639577	A	20000814	<--	
WO 2001-US41674	W	20010813	<--	

AB The present invention is a multi-bit nonvolatile memory and its method of fabrication. According to the present invention a Si channel body having a 1st and 2nd channel surface is formed. A charge storage medium is formed adjacent to the 1st channel surface and a 2nd charge storage medium is formed adjacent to the 2nd channel surface. A 1st control gate is formed adjacent to the 1st charge storage medium adjacent to the 1st channel storage medium adjacent to the 1st channel surface and a 2nd control gate is formed adjacent to the 2nd charge storage medium adjacent to the 2nd surface. According to the 2nd aspect of the present invention, a transistor is provided that has a source, a channel, a drain, and a plurality of gates where the channel current flows vertically between the source and drain. According to a 3rd embodiment of the present invention, a memory element is formed using a transistor that has a read current that flows in a direction perpendicular to a substrate in or over which the transistors form. The transistor has a charge storage medium for storing its state. Multiple control gates address the transistor.

IC ICM H01L0027-115
ICS H01L0021-8246
CC 76-3 (Electric Phenomena)
IT Films
(elec. conductive; method of fabrication of multigate semiconductor device with vertical channel current)
IT Electric conductors
(films; method of fabrication of multigate semiconductor device with vertical channel current)
IT Dielectric films
Epitaxial films
Ion implantation
MOS devices
Nonvolatile memory devices
Semiconductor device fabrication
(method of fabrication of multigate semiconductor device with vertical channel current)
IT 7803-62-5, Silane, processes
RL: CPS (Chemical process); NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(CVD silicon nanocrystals; method of fabrication of multigate semiconductor device with vertical channel current)
IT 7631-86-9, Silica, processes 12033-89-5, Silicon nitride, processes
RL: CPS (Chemical process); DEV (Device component use); PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(ONO composite dielec. film; method of fabrication of multigate semiconductor device with vertical channel current)
IT 11104-62-4, Cobalt silicide 12738-91-9, Titanium silicide
RL: DEV (Device component use); USES (Uses)
(elec. conductor; method of fabrication of multigate semiconductor device with vertical channel current)
IT 7440-21-3, Silicon, processes
RL: CPS (Chemical process); DEV (Device component use); PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(substrate, epitaxial film; method of fabrication of multigate semiconductor device with vertical channel current)
IT 7803-62-5, Silane, processes
RL: CPS (Chemical process); NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(CVD silicon nanocrystals; method of fabrication of multigate semiconductor device with vertical channel current)
RN 7803-62-5 HCAPLUS
CN Silane (CA INDEX NAME)

IT 11104-62-4, Cobalt silicide
RL: DEV (Device component use); USES (Uses)
(elec. conductor; method of fabrication of multigate semiconductor device with vertical channel current)
RN 11104-62-4 HCAPLUS
CN Cobalt silicide (CA INDEX NAME)

Component	Ratio	Component Registry Number
Co	x	7440-48-4
Si	x	7440-21-3

RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L95 ANSWER 12 OF 28 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 2002:138842 HCAPLUS Full-text
DN 136:192048
TI Procedure for the deposition of thin layers by chemical vapor deposition
IN Saenger, Annette
PA Infineon Technologies Ag, Germany
SO Ger., 6 pp.
CODEN: GWXXAW
DT Patent
LA German
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 10063717	C1	20020221	DE 2000-10063717	20001220 <--
	NL 1019553	A1	20020621	NL 2001-1019553	20011212 <--
	NL 1019553	C2	20020906		
	US 2002012338	A1	20020912	US 2001-34053	20011220 <--
	US 6767581	B2	20040727		
PRAI	DE 2000-10063717	A	20001220	<--	

AB A procedure for the deposition of thin layers by chemical vapor deposition is described, whereby an effective quantity of nitroxyl radicals of the structure R1R2NO is added to a gas flow containing the materials to can be deposited. The the radical structure, R1 and R2 stand for equivalent or different alkyl, alkenyl, alkynyl, acyl, or aryl residues with or without hetero atoms. Together, R1 and R2 can also represent a structure -CR3R4-CR5R6-CR7R8-CR9R10-CR11R12, where R3, R4, R5, R6, R7, R8, R9, R10, R11, R12 stand for equivalent or different alkyl, alkenyl, alkynyl, acyl, or aryl residues with or without hetero atoms.
IC ICM C23C0016-452
CC 75-1 (Crystallography and Liquid Crystals)
Section cross-reference(s): 76
IT Dielectric films
Semiconductor materials
(formed by CVD; procedure for deposition of thin layers by chemical vapor deposition)
IT 1314-61-0P, Tantala 1344-28-1P, Alumina, preparation 7440-25-7P, Tantalum, preparation 7440-33-7P, Tungsten, preparation 7440-48-4P, Cobalt, preparation 7631-86-9P, Silica, preparation 12017-11-7P, Cobalt silicide (CoSi) 12033-89-5P, Silicon nitride, preparation 12058-38-7P, Tungsten nitride (WN) 12504-61-9P, Tantalum silicide (TaSi) 12627-41-7P, Tungsten silicide
RL: SPN (Synthetic preparation); TEM (Technical or engineered material use); PREP (Preparation); USES (Uses)
(formed by CVD; procedure for deposition of thin layers by chemical vapor deposition)
IT 4109-96-0, Dichlorosilane 7664-41-7, Ammonia, reactions 7783-82-6, Tungsten hexafluoride
RL: RCT (Reactant); RACT (Reactant or reagent)
(vapor deposition precursor; procedure for deposition of thin layers by

chemical vapor deposition)
IT 7440-48-4P, Cobalt, preparation 12017-11-7P,
Cobalt silicide (CoSi)
RL: SPN (Synthetic preparation); TEM (Technical or engineered material use); PREP (Preparation); USES (Uses)
(formed by CVD; procedure for deposition of thin layers by chemical vapor deposition)
RN 7440-48-4 HCAPLUS
CN Cobalt (CA INDEX NAME)

RN 12017-11-7 HCAPLUS
CN Cobalt silicide (CoSi) (6CI, 8CI, 9CI) (CA INDEX NAME)

IT 4109-96-0, Dichlorosilane
RL: RCT (Reactant); RACT (Reactant or reagent)
(vapor deposition precursor; procedure for deposition of thin layers by chemical vapor deposition)
RN 4109-96-0 HCAPLUS
CN Silane, dichloro- (CA INDEX NAME)

RE.CNT 1 THERE ARE 1 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L95 ANSWER 13 OF 28 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 2002:107878 HCAPLUS Full-text
DN 136:176436
TI Method of producing doped polysilicon layers and polysilicon layered structures, and method of structuring layers, and layered structures which comprise polysilicon layers
IN Dreybrodt, Joerg; Drescher, Dirk; Zedlitz, Ralf; Wege, Stephan
PA Infineon Technologies AG, Germany
SO U.S. Pat. Appl. Publ., 18 pp., Cont.-in-part of U.S. Ser. No. 26,659, abandoned.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 20020016044	A1	20020207	US 2001-884188	20010619 <--
	US 6479373	B2	20021112		
	DE 19706783	A1	19980827	DE 1997-19706783	19970220 <--
	US 20030017684	A1	20030123	US 2002-226764	20020823 <--
	US 6693022	B2	20040217		

PRAI DE 1997-19706783 A 19970220 <--
US 1998-26659 B2 19980220 <--
US 2001-884188 A3 20010619 <--

AB Doped polysilicon layers and layered polysilicon structures are produced, and the layers and layered structures are structured. The doping is distinguished by the fact that the doping compound is added as a process gas during the CVD of the polysilicon to define the doping profile. The feed of dopant to the process gas is stopped toward the end of the vapor deposition, with the result that a boundary layer of undoped Si is deposited. As a result, a favorable surface quality and better adhesion to a neighboring layer is obtained. The structuring process comprises an ≥3-step etching process in which a F containing gas is used for etching in a 1st step, a Cl-containing gas is used for etching in a 2nd step and a Br-containing gas is used for etching in a 3rd step. The invention also encompasses wafers and semiconductor chips produced with the novel doping and/or structuring method.

IC ICM H01L0021-336
INCL 438305000
CC 76-3 (Electric Phenomena)
IT Dielectric films
Doping
Electric insulators
Etching
Semiconductor materials
(method of producing doped polysilicon layers and polysilicon layered structures, and method of structuring layers, and layered structures which comprise polysilicon layers)
IT 7439-98-7, Molybdenum, uses 7440-25-7, Tantalum, uses 7440-32-6, Titanium, uses 7440-33-7, Tungsten, uses 7440-48-4, Cobalt, uses 11104-62-4, Cobalt silicide
11104-85-1, Molybdenum silicide 12627-41-7, Tungsten silicide
12738-91-9, Titanium silicide 52953-72-7, Tantalum silicide
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(method of producing doped polysilicon layers and polysilicon layered structures, and method of structuring layers, and layered structures which comprise polysilicon layers)
IT 7803-62-5, Silane, reactions
RL: RCT (Reactant); RACT (Reactant or reagent)
(vapor deposition precursor; method of producing doped polysilicon layers and polysilicon layered structures, and method of structuring layers, and layered structures which comprise polysilicon layers)
IT 7440-48-4, Cobalt, uses 11104-62-4, Cobalt silicide
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(method of producing doped polysilicon layers and polysilicon layered structures, and method of structuring layers, and layered structures which comprise polysilicon layers)
RN 7440-48-4 HCAPLUS
CN Cobalt (CA INDEX NAME)

Co

RN 11104-62-4 HCAPLUS
CN Cobalt silicide (CA INDEX NAME)

Component	Ratio	Component

		Registry Number
Co	x	7440-48-4
Si	x	7440-21-3

IT 7803-62-5, Silane, reactions
RL: RCT (Reactant); RACT (Reactant or reagent)
(vapor deposition precursor; method of producing doped polysilicon layers and polysilicon layered structures, and method of structuring layers, and layered structures which comprise polysilicon layers)
RN 7803-62-5 HCAPLUS
CN Silane (CA INDEX NAME)

SiH4

L95 ANSWER 14 OF 28 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 2001:875230 HCAPLUS Full-text
DN 136:14138
TI Method of forming copper dual damascene structure with a tungsten blocking layer formed on a silicide layer
IN Lin, Chien-hsing
PA United Microelectronics Corp., Taiwan
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6326306	B1	20011204	US 2001-783872	20010215 <--
PRAI US 2001-783872		20010215 <--		

AB A method of forming a Cu dual damascene structure is disclosed. The method comprises forming Cu lead lines and Cu contacts simultaneously and selectively depositing W layers on silicide layers formed on the active regions to complete the Cu dual damascene structure and avoid the diffusion of Cu into the active regions.
IC ICM H01L0021-44
INCL 438687000
CC 76-3 (Electric Phenomena)
IT Contact holes
Dielectric films
Diffusion barrier
Electric contacts
Electric insulators
Electrodeposition
Interconnections, electric
Semiconductor device fabrication
(method of forming copper dual damascene structure with a tungsten blocking layer formed on a silicide layer)
IT 7440-21-3, Silicon, uses 7440-33-7, Tungsten, uses 7440-50-8, Copper, uses 11104-62-4, Cobalt silicide 12738-91-9, Titanium silicide 124221-30-3
RL: DEV (Device component use); USES (Uses)
(method of forming copper dual damascene structure with a tungsten blocking layer formed on a silicide layer)
IT 7783-82-6, Tungsten hexafluoride 7803-62-5, Silane, reactions

RL: RCT (Reactant); RACT (Reactant or reagent)
(vapor deposition precursor; method of forming copper dual damascene structure with a tungsten blocking layer formed on a silicide layer)
IT 11104-62-4, Cobalt silicide
RL: DEV (Device component use); USES (Uses)
(method of forming copper dual damascene structure with a tungsten blocking layer formed on a silicide layer)
RN 11104-62-4 HCAPLUS
CN Cobalt silicide (CA INDEX NAME)

Component	Ratio	Component Registry Number
Co	x	7440-48-4
Si	x	7440-21-3

IT 7803-62-5, Silane, reactions
RL: RCT (Reactant); RACT (Reactant or reagent)
(vapor deposition precursor; method of forming copper dual damascene structure with a tungsten blocking layer formed on a silicide layer)
RN 7803-62-5 HCAPLUS
CN Silane (CA INDEX NAME)

SiH4

RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L95 ANSWER 15 OF 28 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 2001:851536 HCAPLUS Full-text
DN 135:379710
TI Polysilicon sidewall with silicide formation to produce high performance MOSFETs
IN Ligon, William A.
PA Advanced Micro Devices, Inc., USA
SO PCT Int. Appl., 21 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI WO 2001088991	A2	20011122	WO 2001-US12359	20010416 <--
WO 2001088991	A3	20020523		
W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW				
RW: GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW, AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR, BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG				
US 6630721	B1	20031007	US 2000-571823	20000516 <--
AU 2001055413	A	20011126	AU 2001-55413	20010416 <--
PRAI US 2000-571823	A	20000516	<--	
WO 2001-US12359	W	20010416	<--	

AB A method is provided for lowering the overall gate resistance of a MOSFET transistor. Sidewalls of a polysilicon gate conductor are surrounded by dielec. sidewall spacers. An upper surface of the dielec. spacers is lower than an upper surface of the polysilicon gate conductor thereby exposing a portion of the sidewalls of the gate. The top of the gate and the exposed portion of the sidewalls may be subjected to a salicidation process. During this process, salicide structures are also formed on junction regions. Therefore, silicide may be simultaneously formed on a substantial portion of the gate and on junction regions thereby providing a gate with lower resistivity without consuming the junction regions during salicidation. A MOSFET transistor having silicide formed on top of a polysilicon gate conductor, on partially exposed sidewalls of the polysilicon gate conductor, and on junction regions in an underlying semiconductor substrate is also provided.

IC ICM H01L0029-00

CC 76-3 (Electric Phenomena)

IT Annealing
MOSFET (transistors)
Rapid thermal annealing
(polysilicon sidewall with silicide formation to produce high performance MOSFETs)

IT Dielectric films
(silica, silicon nitride; polysilicon sidewall with silicide formation to produce high performance MOSFETs)

IT 7440-32-6, Titanium, processes 7440-48-4, Cobalt, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(deposited over substrate; polysilicon sidewall with silicide formation to produce high performance MOSFETs)

IT 7803-62-5, Silane, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(polysilicon CVD; polysilicon sidewall with silicide formation to produce high performance MOSFETs)

IT 78-10-4, TEOS 11104-62-4, Cobalt silicide
12738-91-9, Titanium silicide
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(polysilicon sidewall with silicide formation to produce high performance MOSFETs)

IT 7440-48-4, Cobalt, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(deposited over substrate; polysilicon sidewall with silicide formation to produce high performance MOSFETs)

RN 7440-48-4 HCAPLUS

CN Cobalt (CA INDEX NAME)

Co

IT 7803-62-5, Silane, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(polysilicon CVD; polysilicon sidewall with silicide formation to produce high performance MOSFETs)

RN 7803-62-5 HCAPLUS

CN Silane (CA INDEX NAME)

SiH4

IT 11104-62-4, Cobalt silicide
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(polysilicon sidewall with silicide formation to produce high performance MOSFETs)
RN 11104-62-4 HCAPLUS
CN Cobalt silicide (CA INDEX NAME)

Component	Ratio	Component Registry Number
Co	x	7440-48-4
Si	x	7440-21-3

RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L95 ANSWER 16 OF 28 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 2001:828130 HCAPLUS Full-text
DN 135:337941
TI Method for gate-drain multilayer structure by liquid phase deposition of silica layer in CMOS fabrication
IN Wu, Shie-Lin
PA Powerchip Semiconductor Corporation, Taiwan
SO Taiwan, 22 pp.
CODEN: TWXXA5
DT Patent
LA Chinese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI TW 383408	B	20000301	TW 1997-86104000	19970328 <--
PRAI TW 1997-86104000		19970328 <--		

AB A method for CMOS transistor multilayer gate-drain structure is disclosed. A field oxide layer is formed on a semiconductor substrate, followed by 1st conductive well, 2nd conductive well, gate electrode and gate oxide layer. A first dielec. layer is formed on top of gate electrode and gate oxide layer to compensate damaged gate oxide layer, followed by a lightly doped drain electrode formation in the 1st conductive well and 2nd conductive well. A plurality of amorphous Si sidewall is formed on both sides of the gate electrode, followed by formation of heavily doped source/drain electrodes and gate electrodes. A liquid phase deposited silicon oxide sidewall is formed on both sides of amorphous Si sidewall. and metal silicide is formed on source/drain electrodes, gate electrode and amorphous Si sidewall which are not covered with on liquid phase deposited Si oxide sidewall. Finally, metal silicide is formed on source/drain electrodes, gate electrode and amorphous Si sidewall which are not covered with on liquid phase deposited Si oxide sidewall.
IC ICM H01L0021-28
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 75
IT MOS devices
(complementary; multilayer gate-drain structure by liquid phase deposition of silica layers in CMOS fabrication)
IT Coating process

(liquid phase; multilayer gate-drain structure by liquid phase deposition of silica layers in CMOS fabrication)
IT Coating materials
(masking; multilayer gate-drain structure by liquid phase deposition of silica layers in CMOS fabrication)
IT Dielectric films
Ion implantation
(multilayer gate-drain structure by liquid phase deposition of silica layers in CMOS fabrication)
IT 7803-62-5, Silane, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(CVD; multilayer gate-drain structure by liquid phase deposition of silica layers in CMOS fabrication)
IT 11105-01-4, Silicon oxynitride
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(dielec. film; multilayer gate-drain structure by liquid phase deposition of silica layers in CMOS fabrication)
IT 11104-62-4, Cobalt silicide 11129-80-9, Platinum silicide 12039-83-7, Titanium disilicide
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(multilayer gate-drain structure by liquid phase deposition of silica layers in CMOS fabrication)
IT 7803-62-5, Silane, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(CVD; multilayer gate-drain structure by liquid phase deposition of silica layers in CMOS fabrication)
RN 7803-62-5 HCAPLUS
CN Silane (CA INDEX NAME)

IT 11104-62-4, Cobalt silicide
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(multilayer gate-drain structure by liquid phase deposition of silica layers in CMOS fabrication)
RN 11104-62-4 HCAPLUS
CN Cobalt silicide (CA INDEX NAME)

Component	Ratio	Component Registry Number
Co	x	7440-48-4
Si	x	7440-21-3

L95 ANSWER 17 OF 28 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 2001:713853 HCAPLUS Full-text
DN 135:250417
TI Method for manufacturing a gate structure incorporating therein aluminum oxide as a gate dielectric to reduce leakage current and lower interface state density
IN Park, Dae-Gyu; Jang, Se-Aug; Lee, Jeong-youb

PA Hyundai Electronics Industries Co., Ltd., S. Korea
SO U.S. Pat. Appl. Publ., 6 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

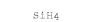
	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE	
PI	US 20010024860	A1	20010927	US 2000-739292	20001219	<--
	US 6524918	B2	20030225			
	KR 2001065161	A	20010711	KR 1999-65030	19991229	<--
PRAI	KR 1999-65030	A	19991229	<--		

AB A method for forming a gate structure begins by preparing a semiconductor substrate provided with an isolation region formed therein. An Al2O3 layer is deposited on top of the semiconductor substrate and then, Si ion plasma doping is carried out. Thereafter, the Al2O3 layer doped with Si ions is annealed in the presence of O gas or nitrous oxide to remove a metallic vacancy in the Al2O3 layer. Subsequently, a conductive layer is formed on top of the Al2O3 layer. Finally, the conductive layer is patterned into the gate structure.

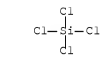
IC ICM H01L0021-336
ICS H01L0021-3205; H01L0021-4763
INCL 438287000
CC 76-3 (Electric Phenomena)
IT Films
(elec. conductive; in method for manufacturing gate structure incorporating therein aluminum oxide as gate dielec. to reduce leakage current and lower interface state d.)
IT Electric conductors
(films; in method for manufacturing gate structure incorporating therein aluminum oxide as gate dielec. to reduce leakage current and lower interface state d.)
IT Coating process
Gate contacts
Oxidation
(method for manufacturing gate structure incorporating therein aluminum oxide as gate dielec. to reduce leakage current and lower interface state d.)
IT 75-24-1, Trimethylaluminum 1184-58-3, Dimethylaluminum chloride 1590-87-0, Silicon hydride (Si2H6) 7446-70-0, Aluminum trichloride, uses 7727-37-9, Nitrogen, uses 7732-18-5, Water, uses 7782-39-0, Deuterium, uses 7803-62-5, Silicon hydride (SiH4), uses 10026-04-7, Silicon chloride (SiCl4) 10028-15-6, Ozone, uses
RL: NUU (Other use, unclassified); USES (Uses)
(in method for manufacturing gate structure incorporating therein aluminum oxide as gate dielec. to reduce leakage current and lower interface state d.)
IT 7440-33-7, Tungsten, processes 7631-86-9, Silica, processes 11104-62-4, Cobalt silicide 11104-85-1, Molybdenum silicide 12033-62-4, Tantalum nitride (TaN) 12058-38-7, Tungsten nitride (WN) 12627-41-7, Tungsten silicide 25583-20-4, Titanium nitride (TiN)
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(in method for manufacturing gate structure incorporating therein aluminum oxide as gate dielec. to reduce leakage current and lower interface state d.)
IT 1590-87-0, Silicon hydride (Si2H6) 7803-62-5, Silicon hydride (SiH4), uses 10026-04-7, Silicon chloride (SiCl4)
RL: NUU (Other use, unclassified); USES (Uses)

(in method for manufacturing gate structure incorporating therein aluminum oxide as gate dielec. to reduce leakage current and lower interface state d.)
RN 1590-87-0 HCAPLUS
CN Disilane (CA INDEX NAME)

RN 7803-62-5 HCAPLUS
CN Silane (CA INDEX NAME)



RN 10026-04-7 HCAPLUS
CN Silane, tetrachloro- (CA INDEX NAME)



IT 11104-62-4, Cobalt silicide
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(in method for manufacturing gate structure incorporating therein aluminum oxide as gate dielec. to reduce leakage current and lower interface state d.)
RN 11104-62-4 HCAPLUS
CN Cobalt silicide (CA INDEX NAME)

Component	Ratio	Component Registry Number
Co	x	7440-48-4
Si	x	7440-21-3

L95 ANSWER 18 OF 28 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 2001:247670 HCAPLUS Full-text
DN 134:274470
TI A nonvolatile memory device with a high work function floating-gate and method of fabrication
IN Mielke, Neal R.; Gill, Manzur
PA Intel Corporation, USA
SO PCT Int. Appl., 52 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1
PATENT NO. KIND DATE APPLICATION NO. DATE

PI	WO 2001024268	A1	20010405	WO 2000-US22784	20000817 <--
	W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM				
	RW: GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW, AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG				
	TW 474013	B	20020121	TW 2000-89119628	20001020 <--
PRAI	US 1999-405553	A	19990924 <--		

AB A nonvolatile memory device and its method of fabrication is described. The elec. erasable nonvolatile memory device of the present invention includes a tunnel dielec. formed on a p-type substrate region. A floating-gate having a work function of >4.1 eV is formed on the tunnel dielec. layer. A dielec. is then formed on the floating-gate. a control gate is then formed on the dielec. over the floating-gate.

IC ICM H01L0027-115
ICS H01L0021-8247; H01L0029-423; H01L0029-49

CC 76-3 (Electric Phenomena)

IT MOS devices
(complementary; fabrication of a nonvolatile memory device with a high work function floating-gate)

IT Epitaxial films
(epitaxial silicon on substrate; fabrication of a nonvolatile memory device with a high work function floating-gate)

IT Dielectric films
(fabrication of a nonvolatile memory device with a high work function floating-gate)

IT Integrated circuits
(fabrication of high d.; fabrication of a nonvolatile memory device with a high work function floating-gate)

IT 7439-98-7, Molybdenum, processes 7440-06-4, Platinum, processes 7440-21-3, Polysilicon, processes 7440-33-7, Tungsten, processes 7440-48-4, Cobalt, processes 11104-62-4, Cobalt silicide 11104-85-1, Molybdenum silicide 11116-16-8, Titanium nitride 12627-41-7, Tungsten silicide 12738-91-9, Titanium silicide 39467-10-2, Nickel silicide
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(floating-gate; fabrication of a nonvolatile memory device with a high work function floating-gate)

IT 76-16-4
RL: NUU (Other use, unclassified); USES (Uses)
(plasma etching pad oxide and dielec. film; fabrication of a nonvolatile memory device with a high work function floating-gate)

IT 7664-41-7, Ammonia, uses 7803-62-5, Silane, uses
RL: NUU (Other use, unclassified); USES (Uses)
(silicon nitride layer by CVD; fabrication of a nonvolatile memory device with a high work function floating-gate)

IT 7440-48-4, Cobalt, processes 11104-62-4, Cobalt silicide
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(floating-gate; fabrication of a nonvolatile memory device with a high work function floating-gate)

RN 7440-48-4 HCAPLUS

CN Cobalt (CA INDEX NAME)

Co

RN 11104-62-4 HCAPLUS
CN Cobalt silicide (CA INDEX NAME)

Component	Ratio	Component Registry Number
Co	x	7440-48-4
Si	x	7440-21-3

IT 7803-62-5, Silane, uses
RL: NUU (Other use, unclassified); USES (Uses)
(silicon nitride layer by CVD; fabrication of a nonvolatile memory device with a high work function floating-gate)
RN 7803-62-5 HCAPLUS
CN Silane (CA INDEX NAME)

SiH4

RE.CNT 9 THERE ARE 9 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L95 ANSWER 19 OF 28 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 2000:605664 HCAPLUS Full-text
DN 133:185817
TI Vapor deposition process for making compound films
IN Desantolo, Anthony Michael; Krisch, Kathleen S.; Mandich, Mary Louise; Opila, Robert Leon, Jr.; Weldon, Marcus
PA Lucent Technologies Inc., USA
SO U.S., 12 pp., Cont.-in-part of U.S. 5,976,623.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6110543	A	20000829	US 1998-197833	19981123 <--
	US 5976623	A	19991102	US 1996-753859	19961203 <--
	US 6264749	B1	20010724	US 1999-333626	19990615 <--
PRAI	US 1996-753859	A2	19961203	<--	

AB The present invention is directed to a process for forming compound films that contain at least three elements. The films are formed on a substrate by directing a gas containing reactant species onto the substrate. The compound film is formed from an interaction between two reactant species. The 3rd element is incorporated into the film as it formed. The 3rd element is different from the other two elements that form the compound film and is H, D, or O. The presence of the 3rd element enhances the properties of the compound film. At least a portion of the substrate remains within the purview of the plasma discharge while the compound film is formed on the substrate.
IC ICM H05H0001-24
ICS C23C0016-00
INCL 427578000

CC 75-1 (Crystallography and Liquid Crystals)
Section cross-reference(s): 76
ST vapor deposition compd film; plasma vapor deposition
IT Silanes
RL: NUU (Other use, unclassified); USES (Uses)
(halosilanes; vapor deposition process for making compound films)
IT Vapor deposition process
(plasma; vapor deposition process for making compound films)
IT Vapor deposition process
(vapor deposition process for making compound films)
IT Silanes
RL: NUU (Other use, unclassified); USES (Uses)
(vapor deposition process for making compound films)
IT Borides
Carbides
Nitrides
Silicides
RL: PEP (Physical, engineering or chemical process); SPN (Synthetic preparation); PREP (Preparation); PROC (Process)
(vapor deposition process for making compound films)
IT 4109-96-0, Dichlorosilane 7664-41-7, Ammonia, processes 7727-37-9, Nitrogen, processes 7803-62-5, Silane, processes 13824-36-7, Difluorosilane
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in deposition of silicon nitride)
IT 7664-41-7D, Ammonia, deuterated, uses
RL: NUU (Other use, unclassified); USES (Uses)
(vapor deposition process for making compound films)
IT 1314-61-0P, Tantalum pentoxide 1344-28-1P, Alumina, processes 11104-62-4P, Cobalt silicide 11104-85-1P, Molybdenum silicide 11105-01-4P, Silicon nitride oxide 11129-80-9P, Platinum silicide 12033-62-4P, Tantalum mononitride 12033-89-5P, Silicon nitride, processes 12045-63-5P, Titanium boride 12070-06-3P, Tantalum carbide 12070-08-5P, Titanium carbide 12627-41-7P, Tungsten silicide 12648-34-9P, Niobium nitride 12738-91-9P, Titanium silicide 13463-67-7P, Titania, processes 25583-20-4P, Titanium mononitride 25658-42-8P, Zirconium nitride 39467-10-2P, Nickel silicide 52953-72-7P, Tantalum silicide
RL: PEP (Physical, engineering or chemical process); SPN (Synthetic preparation); PREP (Preparation); PROC (Process)
(vapor deposition process for making compound films)
IT 4109-96-0, Dichlorosilane 7803-62-5, Silane, processes 13824-36-7, Difluorosilane
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in deposition of silicon nitride)
RN 4109-96-0 HCAPLUS
CN Silane, dichloro- (CA INDEX NAME)

RN 7803-62-5 HCAPLUS
CN Silane (CA INDEX NAME)

SiH_4

RN 13824-36-7 HCAPLUS
CN Silane, difluoro- (6CI, 7CI, 8CI, 9CI) (CA INDEX NAME)

$F-SiH_2-F$

IT 11104-62-4P, Cobalt silicide
RL: PEP (Physical, engineering or chemical process); SPN (Synthetic preparation); PREP (Preparation); PROC (Process)
(vapor deposition process for making compound films)
RN 11104-62-4 HCAPLUS
CN Cobalt silicide (CA INDEX NAME)

Component	Ratio	Component Registry Number
Co	x	7440-48-4
Si	x	7440-21-3

RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L95 ANSWER 20 OF 28 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 2000:381698 HCAPLUS Full-text
DN 132:355744
TI Method of filling contact holes and wiring grooves of a semiconductor device
IN Wada, Junichi; Sakata, Atsuko; Katata, Tomio; Usui, Takamasa; Hasunuma, Masahiko; Shibata, Hideki; Kaneko, Hisashi; Hayasaka, Nobuo; Okumura, Katsuya
PA Kabushiki Kaisha Toshiba, Japan
SO U.S., 106 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6071810	A	20000606	US 1997-997328	19971223 <--
	JP 10189495	A	19980721	JP 1996-344264	19961224 <--
	JP 3488586	B2	20040119		
	JP 10242279	A	19980911	JP 1997-350382	19971219 <--
	JP 4149546	B2	20080910		
	US 20020192938	A1	20021219	US 2002-189598	20020708 <--
	US 6673704	B2	20040106		
	US 20040043602	A1	20040304	US 2003-650974	20030829 <--
	US 6946387	B2	20050920		
PRAI	JP 1996-344264	A	19961224	<--	
	JP 1996-344265	A	19961224	<--	
	JP 1997-350382	A	19971219	<--	
	US 1997-997328	A3	19971223	<--	
	US 2000-556961	A3	20000421	<--	
	US 2002-189598	A3	20020708	<--	

AB A method of manufacturing semiconductor device which comprises the steps of forming an insulating film on an Si substrate provided with a wiring layer, forming a contact hole connected to the wiring layer and a wiring groove in the insulating film, filling the contact hole with an Si film, successively forming an Al film and a Ti film all over the substrate,. Performing a heat treatment thereby to substitute the Al film for the Ti film, and to allow the Si film to be absorbed by the Ti film, whereby filling the contact hole and wiring groove with the Al film, and removing a Ti/Ti silicide which is consisting of Ti silicide formed through the absorption of the Si film by the Ti film and a superfluous Ti, whereby filling the contact hole with an Al plug and filling the wiring groove with an Al wiring.

IC ICM H01L0021-44

INCL 438635000

CC 76-3 (Electric Phenomena)

IT Dielectric films
Heat treatment
Photolithography
Shadow masks
Siliconizing
Sputtering
(in method of filling contact holes and wiring grooves of semiconductor device)

IT 1333-74-0, Hydrogen, uses 7664-41-7, Ammonia, uses 7727-37-9, Nitrogen, uses
RL: NUU (Other use, unclassified); USES (Uses)
(heating atmospheric; in method of filling contact holes and wiring grooves of semiconductor device)

IT 7429-90-5, Aluminum, processes 7440-03-1, Niobium, processes
7440-32-6, Titanium, processes 7440-33-7, Tungsten, processes
7440-48-4, Cobalt, processes 7440-50-8, Copper, processes 7440-56-4, Germanium, processes 7631-86-9, Silica, processes
11104-62-4, Cobalt silicide 11148-21-3 12670-31-4
12713-29-0 25583-20-4, Titanium mononitride 108729-83-5, Tungsten silicide nitride 270075-99-5, Bismuth, copper, tungsten
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in method of filling contact holes and wiring grooves of semiconductor device)

IT 1590-87-0, Disilane 19287-45-7, Diborane
RL: NUU (Other use, unclassified); USES (Uses)
(in method of filling contact holes and wiring grooves of semiconductor device)

IT 7440-48-4, Cobalt, processes 11104-62-4, Cobalt silicide
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in method of filling contact holes and wiring grooves of semiconductor device)

RN 7440-48-4 HCAPLUS

CN Cobalt (CA INDEX NAME)

Co

RN 11104-62-4 HCAPLUS

CN Cobalt silicide (CA INDEX NAME)

Component	Ratio	Component

		Registry Number
Co	x	7440-48-4
Si	x	7440-21-3

IT 1590-87-0, Disilane
RL: NUU (Other use, unclassified); USES (Uses)
(in method of filling contact holes and wiring grooves of semiconductor device)
RN 1590-87-0 HCAPLUS
CN Disilane (CA INDEX NAME)

H3Si—SiH3

RE.CNT 9 THERE ARE 9 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L95 ANSWER 21 OF 28 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 2000:130102 HCAPLUS Full-text
DN 132:174434
TI Manufacture of semiconductor device characterized by etching stopper in formation of self-aligned contact hole
IN Mine, Toshiyuki; Sato, Hidenoro; Ushiyama, Masahiro; Yoshigami, Jiro
PA Hitachi, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2000058483	A	20000225	JP 1998-221323	19980805 <--
PRAI JP 1998-221323		19980805 <--		

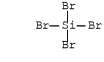
AB The reliability of a MOS transistor having a B-doped poly-Si gate electrode deteriorates, if a Si3N4 film prepared by CVD using Si hydride is used as the etching stopper in the manufacture of a SAC (self-aligned contact-hole), because of the H contained in the S3N4 film. To prevent the trouble (i.e., to decrease the amount of H in the Si3N4 film), Si halides (e.g., SiF4, SiCl4, SiBr4, or SiI4) and N2 gas are used as a raw material instead of a Si hydride in CVD. The H concentration in the Si3N4 film becomes ≤1 + 1021 atoms/cm3.
IC ICM H01L0021-283
ICS H01L0021-28; H01L0021-318
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 75
IT 7631-86-9, Silica, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(film, etching stopper involving; formation of self-aligned contact hole by using silicon nitride etching stopper formed by CVD of silicon halide and nitrogen)
IT 7727-37-9, Nitrogen, processes 7783-61-1, Silicon tetrafluoride 7789-66-4, Silicon tetrabromide 10026-04-7, Silicon tetrachloride 12033-89-5, Silicon nitride, processes 13465-84-4, Silicon tetraiodide
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(formation of self-aligned contact hole by using silicon nitride etching stopper formed by CVD of silicon halide and nitrogen)
IT 7440-33-7, Tungsten, uses 11104-62-4, Cobalt silicide

12627-41-7, Tungsten silicide 12738-91-9, Titanium silicide
25583-20-4, Titanium nitride 37359-53-8, Tungsten nitride 52953-72-7,
Tantalum silicide
RL: TEM (Technical or engineered material use); USES (Uses)
(formation of self-aligned contact hole by using specified etching
stopper with keeping reliability of silicon gate electrode involving)

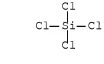
IT 7783-61-1, Silicon tetrafluoride 7789-66-4, Silicon
tetrabromide 10026-04-7, Silicon tetrachloride
13465-84-4, Silicon tetraiodide
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(formation of self-**aligned** contact hole by using silicon nitride
etching stopper formed by CVD of silicon halide and nitrogen)

RN 7783-61-1 HCAPLUS
CN Silane, tetrafluoro- (CA INDEX NAME)

RN 7789-66-4 HCAPLUS
CN Silane, tetrabromo- (CA INDEX NAME)



RN 10026-04-7 HCAPLUS
CN Silane, tetrachloro- (CA INDEX NAME)



RN 13465-84-4 HCAPLUS
CN Silane, tetraiodo- (CA INDEX NAME)

IT 11104-62-4, Cobalt silicide
RL: TEM (Technical or engineered material use); USES (Uses)
(formation of self-aligned contact hole by using specified etching

stopper with keeping reliability of silicon gate electrode involving)
RN 11104-62-4 HCAPLUS
CN Cobalt silicide (CA INDEX NAME)

Component	Ratio	Component Registry Number
Co	x	7440-48-4
Si	x	7440-21-3

L95 ANSWER 22 OF 28 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 1999:538007 HCAPLUS Full-text
DN 131:152688
TI Method of fabricating a buried reservoir capacitor structure for high-density dynamic random access memory (DRAM) circuits
IN Lu, Chih-yuan; Sung, Janmye
PA Vanguard International Semiconductor Corporation, Taiwan
SO U.S., 10 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 5943581	A	19990824	US 1997-964808	19971105 <--
PRAI US 1997-964808		19971105 <--		

AB An improved DRAM cell using a novel buried reservoir capacitor is achieved. The method forms an array of N+ doped regions in a substrate. P-wells are formed in an epitaxy layer on the substrate. A field oxide (FOX) is formed surrounding the device areas aligned over the N+ regions. Holes are etched in the epi layer to the N+ regions, and a selective wet etch removes the N+ doped regions to form cavities. A thin dielec. layer is deposited on the cavity walls, and an N+ polysilicon layer is deposited and polished back to form the buried reservoir capacitors. The N+ polysilicon in the holes forms the capacitor node contacts for the FETs in the device areas. The array of DRAM cells is completed by growing a gate oxide, depositing and patterning a 1st polycide layer to form FET gate electrodes on the device areas over the capacitors, thereby providing increased capacitance while reducing the cell area. Lightly doped source/drain (LDD) areas, sidewall spacers and heavily doped source/drain contacts are formed for the FETs. A node strap is formed between one source/drain contact and the node contact to make good elec. contact. An insulating layer is deposited having bit line contact holes, and a 2nd polycide layer is patterned to form the bit lines for the DRAM.
IC ICM H01L0021-8242
ICS H01L0021-70
INCL 438386000
CC 76-3 (Electric Phenomena)
IT Contact holes
Doping
Electric contacts
Epitaxial films
Epitaxy
Etching
Photolithography
Polycrystalline films
Vapor phase epitaxy
(in method of fabricating buried reservoir capacitor structure for high-d. DRAM circuits)
IT MOS capacitors

Semiconductor device fabrication
(method of fabricating buried reservoir capacitor structure for high-d. DRAM circuits)
IT Field effect transistors
Gate contacts
(method of fabricating buried reservoir capacitor structure for high-d. DRAM circuits with)
IT 11104-62-4, Cobalt silicide 12738-91-9, Titanium silicide 25583-20-4, Titanium nitride
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(node strap; in method of fabricating buried reservoir capacitor structure for high-d. DRAM circuits)
IT 4109-96-0, Dichlorosilane
RL: RCT (Reactant); RACT (Reactant or reagent)
(silicon precursor; in method of fabricating buried reservoir capacitor structure for high-d. DRAM circuits)
IT 11104-62-4, Cobalt silicide
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(node strap; in method of fabricating buried reservoir capacitor structure for high-d. DRAM circuits)
RN 11104-62-4 HCAPLUS
CN Cobalt silicide (CA INDEX NAME)

Component	Ratio	Component Registry Number
Co	x	7440-48-4
Si	x	7440-21-3

IT 4109-96-0, Dichlorosilane
RL: RCT (Reactant); RACT (Reactant or reagent)
(silicon precursor; in method of fabricating buried reservoir capacitor structure for high-d. DRAM circuits)
RN 4109-96-0 HCAPLUS
CN Silane, dichloro- (CA INDEX NAME)

RE.CNT 14 THERE ARE 14 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L95 ANSWER 23 OF 28 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 1996:318768 HCAPLUS Full-text
DN 124:356333
OREF 124:65909a,65912a
TI Metal patterning method
IN Nakano, Hiroyuki
PA Sony Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 15 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 5

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

PI JP 08051058 A 19960220 JP 1994-186184 19940808 <--
JP 3557250 B2 20040825
US 5670297 A 19970923 US 1995-556426 19951109 <--
PRAI JP 1991-360521 A 19911230 <--
JP 1991-360523 A 19911230 <--
JP 1992-87911 A 19920311 <--
JP 1992-87912 A 19920311 <--
JP 1992-244314 A 19920820 <--
JP 1992-316073 A 19921031 <--
JP 1992-359750 A 19921229 <--
US 1992-998743 B2 19921230 <--
US 1993-175299 A2 19931229 <--
JP 1994-186184 A 19940808 <--

AB In the method, comprising forming a reflection-preventing film (A) on an underlayer support containing a metal silicide film (B), forming a resist film (C) on B, patterning C by photolithog. process, and etching B with the mask of patterned C, the optical constant and film thickness of A are decided corresponding to the kind of B so that the standing wave effect might be min. In the method, comprising forming the base metal film on the support so that it might be contacted with Si partially and heating it, forming A and C on it, patterning C, etching the metal film with patterned C, and heating the metal film to form the silicide film, the optical constant and film thickness of A are decided corresponding to the kind of the metal film so that the standing wave effect might be min. In the method, comprising forming A on an underlayer support having a W film (via an interlayer film) forming C on it, patterning C, and etching the W film (or the interlayer film) with patterned C, the optical constant and film-thickness of A are decided corresponding to the W film so that the standing wave effect might be min. The film A may be SiOxNy:H or SixNy, formed by CVD or (reactive) sputtering. The patterning method improves the resolution of line width of the metal film.

IC ICM H01L0021-027
ICS H01L0021-3205; H01L0021-3213

CC 74-13 (Radiation Chemistry, Photochemistry, and Photographic and Other Reprographic Processes)
Section cross-reference(s): 76

ST metal silicide patterning photolithog; titanium cobalt silicide patterning photolithog; platinum nickel silicide patterning photolithog; standing wave effect metal patterning

IT 7664-41-7, Ammonia, uses 7727-37-9, Nitrogen, uses 7803-62-5, Silane, uses 10102-43-9, Nitrogen oxide (NO), uses
RL: TEM (Technical or engineered material use); USES (Uses)
(CVD source; metal patterning method by controlling line width with high accuracy)

IT 7631-86-9, Silicon dioxide, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(interlayer film; metal patterning method by controlling line width with high accuracy)

IT 12017-12-8, Cobalt silicide (CoSi2) 12035-57-3, Nickel silicide (NiSi) 12039-83-7, Titanium silicide (TiSi2) 12137-83-6, Platinum silicide (PtSi)
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(metal patterning method by controlling line width with high accuracy)

IT 11105-01-4, Silicon nitride oxide 12033-89-5, Silicon nitride, processes
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(reflection-preventing film; metal patterning method by controlling line width with high accuracy)

IT 7440-02-0, Nickel, processes 7440-06-4, Platinum, processes 7440-32-6,

Titanium, processes 7440-48-4, Cobalt, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(silicide-forming metal; metal patterning method by controlling line width with high accuracy)
IT 7440-33-7, Tungsten, processes
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(substrate-coating layer; metal patterning method by controlling line width with high accuracy)
IT 7803-62-5, Silane, uses
RL: TEM (Technical or engineered material use); USES (Uses)
(CVD source; metal patterning method by controlling line width with high accuracy)
RN 7803-62-5 HCAPLUS
CN Silane (CA INDEX NAME)

IT 12017-12-8, Cobalt silicide (CoSi2)
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(metal patterning method by controlling line width with high accuracy)
RN 12017-12-8 HCAPLUS
CN Cobalt silicide (CoSi2) (CA INDEX NAME)

IT 7440-48-4, Cobalt, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(silicide-forming metal; metal patterning method by controlling line width with high accuracy)
RN 7440-48-4 HCAPLUS
CN Cobalt (CA INDEX NAME)

L95 ANSWER 24 OF 28 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 1996:39057 HCAPLUS Full-text
DN 124:133182
OREF 124:24459a,24462a
TI Semiconductor device including metal silicide layer and its manufacture
IN Tsutsumi, Toshiaki; Maekawa, Kazuyoshi
PA Mitsubishi Electric Corp, Japan
SO Jpn. Kokai Tokkyo Koho, 10 pp.
CODEN: JKXXAF
DT Patent
LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 07283168	A	19951027	JP 1994-77246	19940415 <--
PRAI	JP 1994-77246		19940415 <--		

AB The semiconductor device is manufactured by (1) depositing metal to form a film on a substrate with selectively exposed Si, (2) heating to form metal-rich silicide layer on the exposed Si, (3) removing unreacted metal, and (4) converting the silicide layer to Si-rich composition by (a) heating under silane-based gas or (b) heating after formation of Si-rich other **metal** silicide layer followed by removal of the 2nd silicide layer. A device having metal silicide formed by self-alignment on exposed Si, which is connected to local circuit comprising other metal silicide layer, of Si content similar chemical stoichiometry, is also claimed.

IC ICM H01L0021-28
ICS H01L0021-324; H01L0021-768; H01L0029-78
; H01L0021-336

CC 76-3 (Electric Phenomena)

ST semiconductor device silicide self alignment; cobalt silicide silicon semiconductor device; connection damage prevention semiconductor device; salicide semiconductor device self alignment; polycide semiconductor device self alignment

IT Semiconductor devices
(manufacture of semiconductor device including formation of metal silicide in self alignment)

IT 12738-91-9, Titanium silicide
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(film; formation of metal silicide in self alignment including conversion of metal-rich silicide to silicon-rich layer by using of)

IT 7803-62-5, Silane, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(gas; formation of metal silicide in self alignment including conversion of metal-rich silicide to silicon-rich layer by using of)

IT 11104-62-4, Cobalt silicide 12017-12-8,
Cobalt silicide (CoSi2)
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(manufacture of semiconductor device including formation of metal silicide in self alignment)

IT 7803-62-5, Silane, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(gas; formation of metal silicide in self alignment including conversion of metal-rich silicide to silicon-rich layer by using of)

RN 7803-62-5 HCAPLUS

CN Silane (CA INDEX NAME)

IT 11104-62-4, Cobalt silicide 12017-12-8,
Cobalt silicide (CoSi2)
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(manufacture of semiconductor device including formation of metal silicide in self alignment)

RN 11104-62-4 HCAPLUS

CN Cobalt silicide (CA INDEX NAME)

Component	Ratio	Component

		Registry Number
Co	x	7440-48-4
Si	x	7440-21-3

RN 12017-12-8 HCAPLUS
CN Cobalt silicide (CoSi2) (CA INDEX NAME)

L95 ANSWER 25 OF 28 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 1995:680695 HCAPLUS Full-text
DN 123:72221
OREF 123:12593a,12596a
TI Silicon film formation
IN Nakajima, Kazuhiro; Ando, Toshio
PA Hitachi Ltd, Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 07014780	A	19950117	JP 1993-153117	19930624 <--
PRAI JP 1993-153117		19930624 <--		

AB Substrates covered by semiconductors (e.g., Si) or metals (e.g., CoSix or Al) are treated such that H atoms lie on the surface, and heated while source gases such as SiH2(CnH2n+1)2 or Si(CnH2n+1)4, and SiH4 are supplied over them.
IC ICM H01L0021-205
ICS C23C0016-24; C23C0016-46
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 75
ST silicon film hydrogen aluminum; cobalt silicide hydrogen silicon film; silane hydrogen silicon film
IT Semiconductor materials
(silicon film formation on substrates covered with)
IT Metals, uses
RL: NUU (Other use, unclassified); USES (Uses)
(silicon film formation on substrates covered with)
IT Films
(silicon film formation on substrates covered with semiconductors or metals)
IT 7664-39-3, Hydrofluoric acid, reactions
RL: RCT (Reactant); RACT (Reactant or reagent)
(hydrogen atom alignment on substrates covered with semiconductors or metals for silicon film formation)
IT 7429-90-5, Aluminum, uses 11104-62-4, Cobalt silicide
RL: NUU (Other use, unclassified); USES (Uses)
(silicon film formation on substrates covered with semiconductors or metals)
IT 7440-21-3P, Silicon, uses
RL: PNU (Preparation, unclassified); TEM (Technical or engineered material use); PREP (Preparation); USES (Uses)
(silicon film formation on substrates covered with

semiconductors or metals)
IT 75-76-3, Tetramethyl silane 1111-74-6, Dimethyl silane
RL: RCT (Reactant); RACT (Reactant or reagent)
(silicon film formation on substrates covered with semiconductors or metals)
IT 1333-74-0, Hydrogen, uses
RL: NUU (Other use, unclassified); USES (Uses)
(silicon film formation on substrates covered with semiconductors or metals containing)
IT 7803-62-5, Silane, reactions
RL: RCT (Reactant); RACT (Reactant or reagent)
(silicon film formation on substrates covered with semiconductors or metals containing)
IT 11104-62-4, Cobalt silicide
RL: NUU (Other use, unclassified); USES (Uses)
(silicon film formation on substrates covered with semiconductors or metals)
RN 11104-62-4 HCAPLUS
CN Cobalt silicide (CA INDEX NAME)

Component	Ratio	Component Registry Number
Co	x	7440-48-4
Si	x	7440-21-3

IT 7803-62-5, Silane, reactions
RL: RCT (Reactant); RACT (Reactant or reagent)
(silicon film formation on substrates covered with semiconductors or metals containing)
RN 7803-62-5 HCAPLUS
CN Silane (CA INDEX NAME)

L95 ANSWER 26 OF 28 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 1994:546811 HCAPLUS Full-text
DN 121:146811
OREF 121:26285a,26288a
TI Manufacture of semiconductor device
IN Tsunenari, Kinji
PA Nippon Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 06089874	A	19940329	JP 1992-213703	19920717 <--
PRAI JP 1992-213703		19920717 <--		

AB In the title manufacture, a high-m.p. metal thin film is formed on a substrate by the following CVD process; (1) sublimating of a Co-containing organic compound, and (2) gas reaction process by forming a high-m.p. metal film on a substrate by allowing the sublimated gas to react with H, NH3, or a gas containing Si; and the formed film is Co. Co silicide film is formed by (1),

and (2) gas reaction process using a gas containing Si as a reactant. The formed films, useful for wirings, have low elec. resistance and are capable of forming smooth-surfaced coatings. Thus, a Co film was formed using Co(C5H7O2)2 and H.

IC ICM H01L0021-285
ICS H01L0021-205

CC 76-3 (Electric Phenomena)
Section cross-reference(s): 75

ST semiconductor device wiring CVD cobalt; silicide cobalt

CVD elec wiring

IT Electric conductors
(cobalt (silicide) sirings, CVD of, in semiconductor devices)

IT Vapor deposition processes
(of cobalt (silicide), for elec. wirings in semiconductor devices)

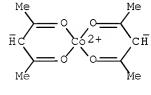
IT 1333-74-0, Hydrogen, reactions 7803-62-5, Silane, uses 14024-48-7
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(in CVD of cobalt (silicide), for elec. wirings in semiconductor devices)

IT 7440-48-4P, Cobalt, preparation 11104-62-4P, Cobalt silicide
RL: PREP (Preparation)
(preparation of, by CVD, for elec. wirings in semiconductor devices)

IT 7803-62-5, Silane, uses 14024-48-7
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(in CVD of cobalt (silicide), for elec. wirings in semiconductor devices)

RN 7803-62-5 HCAPLUS
CN Silane (CA INDEX NAME)

RN 14024-48-7 HCAPLUS
CN Cobalt, bis(2,4-pentanedionato-κO2,κO4)-, (SP-4-1)- (CA INDEX NAME)



IT 7440-48-4P, Cobalt, preparation 11104-62-4P, Cobalt silicide
RL: PREP (Preparation)
(preparation of, by CVD, for elec. wirings in semiconductor devices)

RN 7440-48-4 HCAPLUS
CN Cobalt (CA INDEX NAME)

Co

RN 11104-62-4 HCAPLUS
CN Cobalt silicide (CA INDEX NAME)

Component	Ratio	Component Registry Number
Co	x	7440-48-4
Si	x	7440-21-3

L95 ANSWER 27 OF 28 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 1989:431722 HCAPLUS Full-text
DN 111:31722
OREF 111:5312a
TI Chemical vapor deposition of cobalt silicide films
IN West, Gary A.; Beeson, Karl W.
PA Allied-Signal, Inc., USA
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 4814294	A	19890321	US 1987-79564	19870730 <--
PRAI US 1987-79564		19870730	<--	

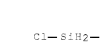
AB Co silicide films are deposited on Si or GaAs from Co carbonyls and **silanes** or halosilanes.
IC ICM H01L0021-285
INCL 437200000
CC 75-1 (Crystallography and Liquid Crystals)
Section cross-reference(s): 76
ST cobalt silicide chem vapor deposition; carbonyl cobalt silane cobalt silicide deposition; halosilane cobalt carbonyl cobalt silicide deposition
IT Semiconductor devices
(chemical vapor deposition of cobalt silicide films for)
IT Epitaxy
(vapor-phase, of cobalt silicide on silicon, from cobalt carbonyls and silanes)
IT 1590-87-0, Disilane 4109-96-0, Dichlorosilane 7783-26-8, Trisilane 7789-57-3, Tribromosilane 7789-66-4, Tetrabromosilane 7803-62-5, Silane, uses and miscellaneous 10025-78-2, Trichlorosilane 10026-04-7, Tetrachlorosilane 13465-71-9, Trifluorosilane 13465-73-1, Monobromosilane 13465-74-2, Bromotrichlorosilane 13465-75-3, Dibromodichlorosilane 13465-76-4, Tribromochlorosilane 13465-78-6, Monochlorosilane 13465-84-4, Tetraiodosilane 13537-33-2, Monofluorosilane 13598-42-0 13768-94-0, Dibromosilane
RL: PRP (Properties)
(chemical vapor deposition of cobalt silicide from cobalt carbonyls and)
IT 10210-68-1 14096-82-3 17786-31-1 48041-08-3

53513-20-5 114885-37-9
RL: PRP (Properties)
(chemical vapor deposition of cobalt silicide from silanes and)
IT 1303-00-0, Gallium arsenide, uses and miscellaneous 7440-21-3, Silicon, uses and miscellaneous
RL: USES (Uses)
(chemical vapor deposition of cobalt silicide on)
IT 12017-11-7, Cobalt monosilicide 12017-12-8, Cobalt disilicide
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(chemical vapor deposition of, from cobalt carbonyls and (halo)silanes)
IT 1590-87-0, Disilane 4109-96-0, Dichlorosilane 7783-26-8, Trisilane 7789-57-3, Tribromosilane 7789-66-4, Tetrabromosilane 7803-62-5, Silane, uses and miscellaneous 10025-78-2, Trichlorosilane 10026-04-7, Tetrachlorosilane 13465-71-9, Trifluorosilane 13465-73-1, Monobromosilane 13465-74-2, Bromotrichlorosilane 13465-75-3, Dibromodichlorosilane 13465-76-4, Tribromochlorosilane 13465-78-6, Monochlorosilane 13465-84-4, Tetraiodosilane 13537-33-2, Monofluorosilane 13598-42-0 13768-94-0, Dibromosilane
RL: PRP (Properties)
(chemical vapor deposition of cobalt silicide from cobalt carbonyls and)
RN 1590-87-0 HCAPLUS
CN Disilane (CA INDEX NAME)

RN 4109-96-0 HCAPLUS
CN Silane, dichloro- (CA INDEX NAME)

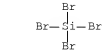
RN 7783-26-8 HCAPLUS
CN Trisilane (CA INDEX NAME)

RN 7789-57-3 HCAPLUS
CN Silane, tribromo- (CA INDEX NAME)



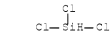
RN 7789-66-4 HCAPLUS

CN Silane, tetrabromo- (CA INDEX NAME)

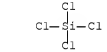


RN 7803-62-5 HCAPLUS
CN Silane (CA INDEX NAME)

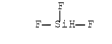
RN 10025-78-2 HCAPLUS
CN Silane, trichloro- (CA INDEX NAME)



RN 10026-04-7 HCAPLUS
CN Silane, tetrachloro- (CA INDEX NAME)

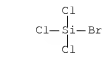


RN 13465-71-9 HCAPLUS
CN Silane, trifluoro- (6CI, 7CI, 8CI, 9CI) (CA INDEX NAME)

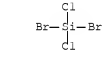


RN 13465-73-1 HCAPLUS
CN Silane, bromo- (6CI, 7CI, 8CI, 9CI) (CA INDEX NAME)

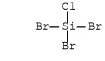
RN 13465-74-2 HCAPLUS
CN Silane, bromotrichloro- (CA INDEX NAME)



RN 13465-75-3 HCAPLUS
CN Silane, dibromodichloro- (6CI, 7CI, 8CI, 9CI) (CA INDEX NAME)

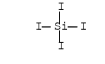


RN 13465-76-4 HCAPLUS
CN Silane, tribromochloro- (6CI, 7CI, 8CI, 9CI) (CA INDEX NAME)



RN 13465-78-6 HCAPLUS
CN Silane, chloro- (CA INDEX NAME)

RN 13465-84-4 HCAPLUS
CN Silane, tetraiodo- (CA INDEX NAME)



RN 13537-33-2 HCAPLUS
CN Silane, fluoro- (CA INDEX NAME)

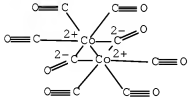
RN 13598-42-0 HCAPLUS
CN Silane, iodo- (6CI, 7CI, 8CI, 9CI) (CA INDEX NAME)

I—SiH3

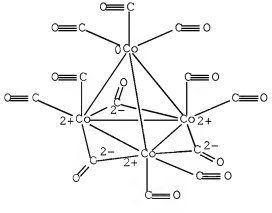
RN 13768-94-0 HCAPLUS
CN Silane, dibromo- (6CI, 7CI, 8CI, 9CI) (CA INDEX NAME)

Br—SiH2—Br

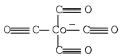
IT 10210-68-1 17786-31-1 48041-08-3
53513-20-5 114885-37-9
RL: PRP (Properties)
(chemical vapor deposition of cobalt silicide from silanes and)
RN 10210-68-1 HCAPLUS
CN Cobalt, di-μ-carbonylhexacarbonyldi-, (Co-Co) (CA INDEX NAME)



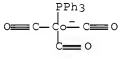
RN 17786-31-1 HCAPLUS
CN Cobalt, tri-μ-carbonylnonacarbonyltetra-, tetrahedro (CA INDEX NAME)



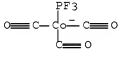
RN 48041-08-3 HCAPLUS
CN Cobaltate(1-), tetracarbonyl-, hydrogen, (T-4)- (9CI) (CA INDEX NAME)



RN 53513-20-5 HCAPLUS
CN Cobaltate(1-), tricarbonyl(triphenylphosphine)-, (T-4)- (CA INDEX NAME)



RN 114885-37-9 HCAPLUS
CN Cobaltate(1-), tricarbonyl(phosphorous trifluoride)-, (T-4)- (CA INDEX NAME)



IT 12017-11-7, Cobalt monosilicide 12017-12-8, Cobalt disilicide
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(chemical vapor deposition of, from cobalt carbonyls and (halo)silanes)
RN 12017-11-7 HCAPLUS
CN Cobalt silicide (CoSi) (6CI, 8CI, 9CI) (CA INDEX NAME)

RN 12017-12-8 HCAPLUS
CN Cobalt silicide (CoSi2) (CA INDEX NAME)

RE.CNT 10 THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L95 ANSWER 28 OF 28 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 1988:465414 HCAPLUS Full-text
DN 109:65414
OREF 109:10795a,10798a
TI Preventing undesirable reactions in a method for fabricating devices using chemical vapor deposition
IN Gallagher, Patrick Kent; Green, Martin Laurence; Levy, Roland Albert
PA American Telephone and Telegraph Co., USA
SO PCT Int. Appl., 32 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI WO 8707763	A1	19871217	WO 1987-US1230	19870527 <--
W: JP, KR				
RW: AT, BE, CH, DE, FR, GB, IT, LU, NL, SE				
EP 268654	A1	19880601	EP 1987-903799	19870527 <--
R: BE, DE, FR, GB, IT, NL				
JP 63503581	T	19881222	JP 1987-503471	19870527 <--
JP 06080682	B	19941012		
CA 1286798	C	19910723	CA 1987-539354	19870610 <--
US 4968644	A	19901106	US 1988-193179	19880505 <--
PRAI US 1986-874475	A	19860616 <--		
WO 1987-US1230	W	19870527 <--		

AB In fabricating a device using methods in which ≥2 materials react to deposit a metal-containing film on a substrate and in which 1 of the reactants also reacts with the substrate, techniques for reducing the rate at which the substrate reacts without reducing the rate of the film-forming reaction are employed. The techniques employed may include increasing the concentration of the products of the undesired reaction (e.g., introducing SiF4 to protect a Si substrate when reacting WF6 and H2 to forming a W layer). Devices are described which include ≥1 n-channel MOS FET which have erosion-free shallow source and drain regions which are provided with contacts which include a metal which penetrates the source and drain regions only slightly, if at all; a diffusion barrier layer or layers may be provided between the device substrate and the metal.

IC ICM H01L0021-285
ICS H01L0023-52
CC 76-3 (Electric Phenomena)
Section cross-reference(s): 75
IT Films
(chemical vapor deposition of, prevention of reactions with substrates in)
IT Transistors
(field-effect, MOS, fabrication of, undesirable reaction prevention in formation of barrier layers for)
IT 11104-62-4 11104-85-1, Molybdenum silicide (unspecified)
11129-80-9 12738-91-9, Titanium silicide (unspecified) 52953-72-7, Tantalum silicide (unspecified)
RL: USES (Uses)
(in MOS FET contact formation)
IT 7783-61-1, Silicon tetrafluoride
RL: USES (Uses)
(in chemical vapor deposition, for prevention of reaction with substrates)
IT 11104-62-4
RL: USES (Uses)
(in MOS FET contact formation)
RN 11104-62-4 HCAPLUS

CN Cobalt silicide (CA INDEX NAME)

Component	Ratio	Component Registry Number
Co	x	7440-48-4
Si	x	7440-21-3

IT 7783-61-1, Silicon tetrafluoride
RL: USES (Uses)
(in chemical vapor deposition, for prevention of reaction with substrates)
RN 7783-61-1 HCAPLUS
CN Silane, tetrafluoro- (CA INDEX NAME)

RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

=> => d bib abs hitstr tot

L104 ANSWER 1 OF 13 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 2007:970307 HCAPLUS Full-text
DN 147:333447
TI Process for forming cobalt-containing materials
IN Ganguli, Seshadri; Chu, Schubert S.; Chang, Mei; Yu, Sang-Ho; Moraes, Kevin; Phan, See-Eng
PA USA
SO U.S. Pat. Appl. Publ., 60pp., Cont.-in-part of U.S. Ser. No. 456,073.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 6

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 20070202254	A1	20070830	US 2007-733929	20070411 <--
	US 20030029715	A1	20030213	US 2001-916234	20010725 <--
	US 20030022487	A1	20030130	US 2002-44412	20020109 <--
	US 6740585	B2	20040525		
	US 20040211665	A1	20041028	US 2004-845970	20040514 <--
	US 20060276020	A1	20061207	US 2006-456073	20060706 <--
	US 7416979	B2	20080826		
	WO 2007121249	A2	20071025	WO 2007-US66442	20070411
	WO 2007121249	A3	20071227		

W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW
RW: AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL, PT, RO, SE, SI, SK, TR, BF,

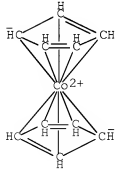
BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG, BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM, AP, EA, EP, OA

	US 20080268635	A1	20081030	US 2008-111930	20080429	<--
	US 20090004850	A1	20090101	US 2008-111923	20080429	<--
	US 20090053426	A1	20090226	US 2008-201976	20080829	<--
	KR 2008110897	A	20081219	KR 2008-727610	20081111	
PRAI	US 2001-916234	B2	20010725	<--		
	US 2002-44412	A1	20020109	<--		
	US 2004-845970	A1	20040514			
	US 2006-791366P	P	20060411			
	US 2006-456073	A2	20060706			
	US 2006-863939P	P	20061101			
	US 2007-733929	A2	20070411			
	WO 2007-US66442	W	20070411			
	US 2008-111923	A2	20080429			
	US 2008-111930	A2	20080429			

AB Embodiments of the invention described herein generally provide methods and apparatuses for forming Co silicide layers, metallic Co layers, and other Co-containing materials. In one embodiment, a method for forming a Co silicide containing material on a substrate is provided which includes exposing a substrate to at least one preclean process to expose a Si-containing surface, depositing a Co silicide material on the Si-containing surface, depositing a metallic Co material on the Co silicide material, and depositing a metallic contact material on the substrate. In another embodiment, a method includes exposing a substrate to at least one preclean process to expose a Si-containing surface, depositing a Co silicide material on the Si-containing surface, expose the substrate to an annealing process, depositing a barrier material on the Co silicide material, and depositing a metallic contact material on the barrier material.

IT 1277-43-6, Bis(cyclopentadienyl) cobalt 1590-87-0, Disilane 7803-62-5, Silane, processes 10210-68-1, Dicobalt octa(carbonyl) 12078-25-0 12078-39-6 12146-91-7, Bis(methylcyclopentadienyl) cobalt 12306-95-5 32825-27-7 32876-13-4 68494-68-8 69393-67-5 73231-01-3 75297-02-8 80848-36-8
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(precursors; process for forming cobalt-containing materials)

RN 1277-43-6 HCAPLUS
CN Cobaltocene (CA INDEX NAME)



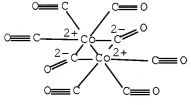
RN 1590-87-0 HCAPLUS
CN Disilane (CA INDEX NAME)

H3Si—SiH3

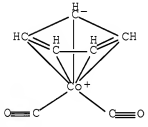
RN 7803-62-5 HCAPLUS
CN Silane (CA INDEX NAME)

SiH4

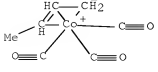
RN 10210-68-1 HCAPLUS
CN Cobalt, di-μ-carbonylhexacarbonyldi-, (Co-Co) (CA INDEX NAME)



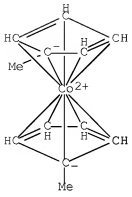
RN 12078-25-0 HCAPLUS
CN Cobalt, dicarbonyl(η5-2,4-cyclopentadien-1-yl)- (CA INDEX NAME)



RN 12078-39-6 HCAPLUS
CN Cobalt, [(1,2,3-η)-2-butenyl]tricarbonyl- (9CI) (CA INDEX NAME)

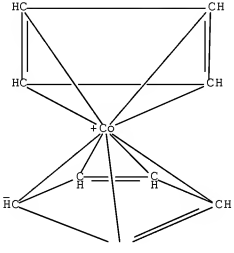


RN 12146-91-7 HCAPLUS
CN Cobaltocene, 1,1'-dimethyl- (9CI) (CA INDEX NAME)



RN 12306-95-5 HCAPLUS
CN Cobalt, (η4-1,3-cyclobutadiene)(η5-2,4-cyclopentadien-1-yl)- (CA INDEX NAME)

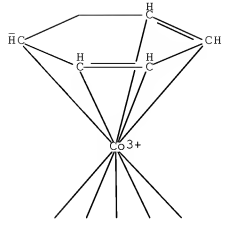
PAGE 1-A



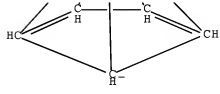
PAGE 2-A

RN 32825-27-7 HCAPLUS
CN Cobalt(1+), [(1,2,3,4,5-η)-2,4-cyclohexadien-1-yl](η5-2,4-cyclopentadien-1-yl)- (9CI) (CA INDEX NAME)

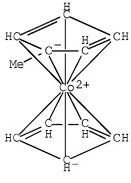
PAGE 1-A



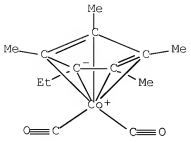
PAGE 2-A



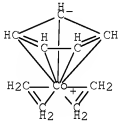
RN 32876-13-4 HCAPLUS
CN Cobaltocene, methyl- (9CI) (CA INDEX NAME)



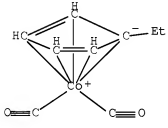
RN 68494-68-8 HCAPLUS
CN Cobalt, dicarbonyl[(1,2,3,4,5-η)-1-ethyl-2,3,4,5-tetramethyl-2,4-cyclopentadien-1-yl]- (9CI) (CA INDEX NAME)



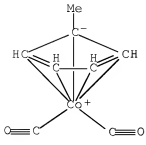
RN 69393-67-5 HCAPLUS
CN Cobalt, (η5-2,4-cyclopentadien-1-yl)bis(η2-ethene)- (CA INDEX NAME)



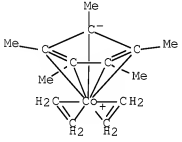
RN 73231-01-3 HCAPLUS
CN Cobalt, dicarbonyl[(1,2,3,4,5-η)-1-ethyl-2,4-cyclopentadien-1-yl]- (9CI) (CA INDEX NAME)



RN 75297-02-8 HCAPLUS
CN Cobalt, dicarbonyl[(1,2,3,4,5-η)-1-methyl-2,4-cyclopentadien-1-yl]- (CA INDEX NAME)



RN 80848-36-8 HCAPLUS
CN Cobalt, bis(η2-ethene)[(1,2,3,4,5-η)-1,2,3,4,5-pentamethyl-2,4-cyclopentadien-1-yl]- (9CI) (CA INDEX NAME)



IT 7440-48-4, Cobalt, formation (nonpreparative) 11104-62-4, Cobalt silicide
RL: FMU (Formation, unclassified); FORM (Formation, nonpreparative)
(process for forming cobalt-containing materials)
RN 7440-48-4 HCAPLUS
CN Cobalt (CA INDEX NAME)

Co

RN 11104-62-4 HCAPLUS
CN Cobalt silicide (CA INDEX NAME)

Component	Ratio	Component Registry Number
Co	x	7440-48-4
Si	x	7440-21-3

L104 ANSWER 2 OF 13 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 2005:207823 HCAPLUS Full-text
DN 142:289382
TI Eliminate bridging between gate and source/drain in cobalt salicidation
IN Shue, Shau-Lin; Wang, Mei-Yun
PA Taiwan Semiconductor Manufacturing Company, Ltd., Taiwan
SO U.S., 12 pp.

CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6864143	B1	20050308	US 2000-489970	20000124 <--
PRAI US 2000-489970		20000124 <--		

AB A new method is provided for the formation of salicided layers for a gate electrode structure. A gate electrode structure is formed, a 1st layer of gate spacers containing oxide is formed on the sidewalls of the gate structure. A 2nd layer of gate spacers is deposited over the 1st layer of gate spacer, this 2nd layer of gate spacer contains SiNx. A layer of Co is deposited over the gate electrode thereby including the gate spacers. The layer of Co is salicided forming reacted and unreacted layers of Co whereby the reacted layers of Co form CoSix on the surface of the gate electrode and the source/drain regions. The unreacted Co and the 2nd gate spacer layer of SiNx are simultaneously removed from the sidewalls of the gate electrode leaving reacted layers of CoSix in place over the surface of the gate structure and the surface of the source/drain regions. The process of removal of the unreacted Co combined with the removal of the layer of SiNx from the sidewalls of the gate electrode removes any possibility of elec. shorts between the points of contact of the gate electrode structure.

IT 11104-62-4P, Cobalt silicide
RL: CPS (Chemical process); DEV (Device component use); PEP (Physical, engineering or chemical process); SPN (Synthetic preparation); PREP (Preparation); PROC (Process); USES (Uses)
(fabrication method for elimination of bridging shorts between gate and source/drain in cobalt salicidation)
RN 11104-62-4 HCAPLUS
CN Cobalt silicide (CA INDEX NAME)

Component	Ratio	Component Registry Number
Co	x	7440-48-4
Si	x	7440-21-3

IT 7440-48-4, Cobalt, processes
RL: CPS (Chemical process); NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(fabrication method for elimination of bridging shorts between gate and source/drain in cobalt salicidation)
RN 7440-48-4 HCAPLUS
CN Cobalt (CA INDEX NAME)

Co

IT 4109-96-0, Dichlorosilane
RL: CPS (Chemical process); NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(silicon nitride precursor; fabrication method for elimination of bridging shorts between gate and source/drain in cobalt salicidation)
RN 4109-96-0 HCAPLUS
CN Silane, dichloro- (CA INDEX NAME)

Cl—SiH2—Cl

RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L104 ANSWER 3 OF 13 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 2004:895828 HCAPLUS Full-text
DN 142:167071
TI Method for manufacturing CMOS transistor
IN Ji, Yeon Hyeok; Jung, Yeong Seok; Mun, Jeong Eon
PA Hynix Semiconductor Inc., S. Korea
SO Repub. Korean Kongkae Taeho Kongbo, No pp. given
CODEN: KRXXA7
DT Patent
LA Korean
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	KR 2001059612	A	20010706	KR 1999-67133	19991230 <--
PRAI	KR 1999-67133		19991230	<--	

AB A method for manufacturing a CMOS transistor is to deposit a cobalt silicide layer on an active region of a semiconductor substrate by the sputtering using SiH4 as reaction gas, to prevent a RC time delay and to reduce diode leakage current, thereby improving elec. characteristics of a semiconductor device. A gate oxide layer and a gate electrode layer are deposited on a semiconductor substrate. The resultant structure is etched and a gate is formed to deposit a spacer layer on its sidewall. A cobalt silicide layer is formed on the gate by impacting Ar gas on a cobalt target in a reaction chamber of the gate so that the scattered Ar gas reacts with SiH4 gas. Selectively, a rapid annealing is implemented after the deposition of the cobalt silicide layer. On the resultant structure is formed a photoresist. The cobalt silicide layer deposited on the gate is removed by a dry-etching, and then residual photoresist is removed.
IT 7440-48-4, Cobalt, processes 7803-62-5, Silicon hydride (SiH4), processes 11104-62-4, Cobalt silicide
RL: CPS (Chemical process); PEP (Physical, engineering or chemical process); PROC (Process)
(manufacturing CMOS transistor by reactive sputtering of cobalt silicide)
RN 7440-48-4 HCAPLUS
CN Cobalt (CA INDEX NAME)

Co

RN 7803-62-5 HCAPLUS
CN Silane (CA INDEX NAME)

SiH4

RN 11104-62-4 HCAPLUS
CN Cobalt silicide (CA INDEX NAME)

Component	Ratio	Component Registry Number
Co	x	7440-48-4
Si	x	7440-21-3

L104 ANSWER 4 OF 13 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 2004:680464 HCAPLUS Full-text
DN 141:182409
TI Two-layer thin vapor deposition masks producing fine patterns and method for their manufacture
IN Nakamura, Kyuzo; Komatsu, Takashi; Tani, Noriaki; Ichinohe, Hiroshi
PA Ulvac Japan, Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2004232025	A	20040819	JP 2003-22211	20030130 <--
PRAI JP 2003-22211		20030130 <--		

AB The masks, useful for manufacture of organic electroluminescent devices, comprise first layers comprising low-heat-expansion metal foils and second layers having predetd. mask patterns and comprising components showing etching characteristic different from that of the metal foils, wherein through holes having opening width increased from the interfaces between the first and the second layers toward vapor deposition sources (diagram given). The method includes preparing laminates comprising the first and the second layers, forming first resist layers on the first layers, patterning the first resist layers, overetching the first layers to give the aforementioned opening width, forming the second resist layers on the second layers, patterning the second resist layers, and etching the second resist layers (flow chart given). Thus, a mask comprising a first layer comprising Fe-Ni-Co alloy and a second layer comprising Ti is exemplified.
IT 7440-48-4, Cobalt, processes 7803-62-5, Silane, processes
RL: PEP (Physical, engineering or chemical process); PYP (Physical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(substrate-facing second layer containing; manufacture of two-layer thin masks having through holes with opening width increased toward vapor deposition sources by photolithog. including overetching)
RN 7440-48-4 HCAPLUS
CN Cobalt (CA INDEX NAME)

RN 7803-62-5 HCAPLUS
CN Silane (CA INDEX NAME)

L104 ANSWER 5 OF 13 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 2004:60088 HCAPLUS Full-text
DN 140:121043
TI Method of fabricating a semiconductor device having a silicon oxide layer and dual spacers
IN Ku, Ja-hum; Lee, Chang-won; Heo, Seong-jun; Sun, Min-chul; Youn, Sun-pil
PA Samsung Electronics Co., Ltd., S. Korea
SO U.S. Pat. Appl. Publ., 15 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE	
PI US 20040014330	A1	20040122	US 2003-612041	20030703	<--
US 7005367	B2	20060228			
KR 2004005330	A	20040116	KR 2002-39834	20020709	<--
TW 220552	B	20040821	TW 2003-92116073	20030613	<--
CN 1471144	A	20040128	CN 2003-148470	20030630	<--
CN 1327496	C	20070718			
JP 2004080011	A	20040311	JP 2003-194052	20030709	<--
US 20060057807	A1	20060316	US 2005-269599	20051109	<--
US 7465617	B2	20081216			
PRAI KR 2002-39834	A	20020709	<--		
US 2003-612041	A1	20030703	<--		

AB The present invention relates to a method of fabricating a semiconductor device that includes a silicon oxide layer, and more particularly, to a method of fabricating a semiconductor device that includes dual spacers that include a silicon oxide layer formed on sidewalls of a gate line patterns. A N atmospheric may be created and maintained in a reaction chamber by supplying a N source gas. A Si source gas and an O source gas may then be supplied to the reaction chamber to deposit a Si oxide layer on a semiconductor substrate, which may include a conductive material layer. A Si nitride layer may then be formed on the Si oxide layer by performing a general CVD process. Next, the Si nitride layer may be etched until the Si oxide layer is exposed. Because of the difference in etching selectivity between Si nitride and Si oxide, portions of the Si nitride layer may remain on sidewalls of the conductive material layer. As a result, dual spacers formed of a Si oxide layer and a Si nitride layer may be formed on the sidewalls.
IT 7440-48-4, Cobalt, uses
RL: DEV (Device component use); USES (Uses)
(device conductive layer; method of fabricating a semiconductor device having a silicon oxide layer and dual spacers)
RN 7440-48-4 HCAPLUS
CN Cobalt (CA INDEX NAME)

Co

IT 4109-96-0, Dichlorosilane 7803-62-5, Silane, reactions
10025-78-2, Trichlorosilane 13465-77-5, Hexachlorodisilane
RL: RCT (Reactant); RACT (Reactant or reagent)
(vapor deposition precursor; method of fabricating a semiconductor device having a silicon oxide layer and dual spacers)
RN 4109-96-0 HCAPLUS

CN Silane, dichloro- (CA INDEX NAME)

RN 7803-62-5 HCAPLUS
CN Silane (CA INDEX NAME)

RN 10025-78-2 HCAPLUS
CN Silane, trichloro- (CA INDEX NAME)

RN 13465-77-5 HCAPLUS
CN Disilane, 1,1,1,2,2,2-hexachloro- (CA INDEX NAME)

RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L104 ANSWER 6 OF 13 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 2002:819585 HCAPLUS Full-text
DN 137:287341
TI Method for the formation of a deep-submicron CMOS with self-aligned silicide contact and extended source/drain contact
IN Wu, Shie-Lin
PA TSMC-Acer Semiconductor Manufacturing Corporation, Taiwan
SO Taiwan, 17 pp.
CODEN: TWXXA5
DT Patent
LA Chinese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI TW 396417	B	20000701	TW 1998-87108786	19980604 <--
PRAI TW 1998-87108786		19980604 <--		

AB This is an oxide layer and a polysilicon layer on the substrate. Then, a silicon nitride layer is formed on the polysilicon layer. Also, etching is proceeded on the undoped polysilicon layer, silicon nitride layer, and oxide layer to form a poly- silicon gate with very short channels. Then thermal annealing is applied to repair damages on the substrate resulted from etching;

a pad oxide layer is formed between the polysilicon gate and the substrate. First, an N-doped amorphous silicon layer is formed on the gate structure and the pad oxide layer, then, source/drain is formed by ion implantation. The N-doped amorphous silicon layer is then transformed into N-doped thermal silica layer. A very shallow extended source/drain contact adjacent to the gate structure is formed simultaneously by using the amorphous silicon layer as a diffusion source. Then the N-doped silica layer is etched back to form a spacer wall. After the shield silicon nitride layer is removed, mental silicide contact can be obtained.

IT 1590-87-0, Disilane
RL: RCT (Reactant); RACT (Reactant or reagent)
(etchant; polysilicon gate in formation of deep-submicron CMOS with self-aligned silicide contact and extended source/drain contact)
RN 1590-87-0 HCAPLUS
CN Disilane (CA INDEX NAME)

IT 7440-48-4, Cobalt, reactions
RL: RCT (Reactant); RACT (Reactant or reagent)
(polysilicon gate in formation of deep-submicron CMOS with self-aligned silicide contact and extended source/drain contact)
RN 7440-48-4 HCAPLUS
CN Cobalt (CA INDEX NAME)

L104 ANSWER 7 OF 13 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 2001:630924 HCAPLUS Full-text
DN 135:188773
TI Gate stack structure for variable threshold voltage
IN Yu, Bin; Adem, Ercan
PA Advanced Micro Devices, Inc., USA
SO U.S., 25 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6281559	B1	20010828	US 1999-261274	19990303 <--
PRAI US 1999-261274		19990303 <--		

AB An ultra-large-scale integrated (ULSI) circuit includes MOSFETs which have different threshold voltages and yet have the same channel characteristics. The MOSFETs include gate structures or gate stacks with a Si and Ge material provided over a seed layer. The seed layer can be a 20-40 Å polysilicon layer. An amorphous Si layer is provided over the Si and Ge material, and a cap layer is provided over the amorphous Si layer. The polysilicon material is implanted with lower concns. of Ge, where lower threshold voltage MOSFETs are required. Over a range of 0-60 concentration of Ge, the threshold voltage can be varied by roughly 240 mV.

IT 7440-48-4, Cobalt, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical

process); PROC (Process); USES (Uses)
(CVD; silicon germanium compound semiconductor gate stack structure for variable threshold voltage in ULSI circuits)
RN 7440-48-4 HCAPLUS
CN Cobalt (CA INDEX NAME)

Co

IT 11104-62-4, Cobalt silicide
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in gate stack; silicon germanium compound semiconductor gate stack structure for variable threshold voltage in ULSI circuits)
RN 11104-62-4 HCAPLUS
CN Cobalt silicide (CA INDEX NAME)

Component	Ratio	Component Registry Number
Co	x	7440-48-4
Si	x	7440-21-3

IT 7803-62-5, Silane, processes
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(low-pressure CVD; silicon germanium compound semiconductor gate stack structure for variable threshold voltage in ULSI circuits)
RN 7803-62-5 HCAPLUS
CN Silane (CA INDEX NAME)

SiH4

RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L104 ANSWER 8 OF 13 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 2000:754460 HCAPLUS Full-text
DN 133:304530
TI Method of manufacturing deep sub-micron CMOS transistors
IN Wu, Shye-Lin
PA Texas Instruments - Acer Incorporated, Taiwan
SO U.S., 9 pp., Cont.-in-part of U.S. 5,930,617.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 5

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6136636	A	20001024	US 1999-291265	19990414 <--
	US 5930617	A	19990727	US 1998-48154	19980325 <--
PRAI	US 1998-48154	A2	19980325	<--	

AB The present invention includes forming N-doped amorphous Si layer on the gate structure and on a pad oxide. Nitride spacers are formed on the side walls of the gate structure. Then, the nitride spacers and the cap nitride are both removed by wet etching. Next, an ion implantation is carried out to implant

dopants into the gate and in the N well. Doped regions for the NMOS device are next formed in the P well by performing a further ion implantation. An oxidation is performed to convert the N-doped amorphous Si layer to a N-doped oxide layer. An ultra-shallow source and drain junctions and the extended source and drain are obtained by using the amorphous Si layer as a diffusion source. Next, N spacers on the side walls of the oxide are formed. The oxide on the top of the gate and uncovered by the spacers are removed during the etching to form spacers. Self-aligned silicide (SALICIDE) and polycide are resp. formed on the exposed substrate and gate.

IT 1590-87-0, Disilane
RL: RCT (Reactant); RACT (Reactant or reagent)
(method of manufacturing deep sub-micron CMOS transistors)
RN 1590-87-0 HCAPLUS
CN Disilane (CA INDEX NAME)

IT 7440-48-4, Cobalt, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(semiconductor structure metal layer; method of manufacturing deep sub-micron
CMOS transistors)
RN 7440-48-4 HCAPLUS
CN Cobalt (CA INDEX NAME)

RE.CNT 9 THERE ARE 9 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L104 ANSWER 9 OF 13 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 1999:482114 HCAPLUS Full-text
DN 131:109901
TI Improved polycide layer for semiconductor device fabrication by doping the metal silicide
IN Ilg, Matthias; Faltermeier, Johnathan; Srinivasan, Radhika
PA Siemens A.-G., Germany; International Business Machines Corp.
SO Eur. Pat. Appl., 8 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE	
PI	EP 932186	A2	19990728	EP 1999-100773	19990116	<--
	EP 932186	A3	19990818			
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO					
	US 6130145	A	20001010	US 1998-10081	19980121	<--
	TW 409296	B	20001021	TW 1999-88100188	19990107	<--
	JP 11265992	A	19990928	JP 1999-10404	19990119	<--
	CN 1230780	A	19991006	CN 1999-101316	19990119	<--
PRAI	US 1998-10081	A	19980121	<--		

AB A reduced metal-rich interface between a poly and metal silicide layer is achieved by in situ doping the metal silicide layer.

IT 11104-62-4P, Cobalt silicide
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); SPN (Synthetic preparation); PREP (Preparation); PROC (Process); USES (Uses)
(improved polycide layer for semiconductor device fabrication by doping metal silicide)

RN 11104-62-4 HCAPLUS
CN Cobalt silicide (CA INDEX NAME)

Component	Ratio	Component Registry Number
Co	x	7440-48-4
Si	x	7440-21-3

IT 1590-87-0, Disilane 4109-96-0, Dichlorosilane
7803-62-5, Silane, reactions
RL: RCT (Reactant); RACT (Reactant or reagent)
(precursor for silicide CVD; improved polycide layer for semiconductor device fabrication by doping metal silicide)

RN 1590-87-0 HCAPLUS
CN Disilane (CA INDEX NAME)

RN 4109-96-0 HCAPLUS
CN Silane, dichloro- (CA INDEX NAME)

RN 7803-62-5 HCAPLUS
CN Silane (CA INDEX NAME)

L104 ANSWER 10 OF 13 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 1998:580010 HCAPLUS Full-text
DN 129:210426
OREF 129:42559a,42562a
TI Preparation of doped polysilicon layers and layered structures and patterning polysilicon-containing layers and layered structures
IN Dreybrodt, Joerg; Drescher, Dirk; Zedlitz, Ralf; Wege, Stephan
PA Siemens A.-G., Germany
SO Ger. Offen., 20 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 19706783	A1	19980827	DE 1997-19706783	19970220 <--
	EP 865074	A2	19980916	EP 1998-101176	19980123 <--
	EP 865074	A3	20000105		
	EP 865074	B1	20080813		
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	JP 10242065	A	19980911	JP 1998-55804	19980220 <--
	JP 4163781	B2	20081008		
	US 20020016044	A1	20020207	US 2001-884188	20010619 <--
	US 6479373	B2	20021112		
	US 20030017684	A1	20030123	US 2002-226764	20020823 <--
	US 6693022	B2	20040217		
	JP 2008182200	A	20080807	JP 2007-318202	20071210 <--
PRAI	DE 1997-19706783	A	19970220	<--	
	JP 1998-55804	A3	19980220	<--	
	US 1998-26659	B2	19980220	<--	
	US 2001-884188	A3	20010619	<--	

AB The dopant compound is used as a process gas in the CVD of polysilicon, and its supply is stopped near the end of the CVD, so that a boundary layer of undoped Si is deposited. Thus a favorable surface quality and improved adhesion to a neighboring layer are achieved. The patterning process includes etching in ≥3 stages, in which in the 1st stage a F-containing gas, in the 2nd stage a Cl-containing gas, and in the 3rd stage a Br-containing gas is used. Wafers and semiconductor chips prepared by these methods are also claimed.

IT 7783-61-1, Silicon fluoride (SiF4)
RL: PEP (Physical, engineering or chemical process); PROC (Process)
(etching by gas mixts. containing; in patterning of doped polysilicon layers)

RN 7783-61-1 HCAPLUS

CN Silane, tetrafluoro- (CA INDEX NAME)

IT 11104-62-4, Cobalt silicide
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(preparation and patterning of doped polysilicon layered structures containing)

RN 11104-62-4 HCAPLUS

CN Cobalt silicide (CA INDEX NAME)

Component	Ratio	Component Registry Number
Co	x	7440-48-4
Si	x	7440-21-3

RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L104 ANSWER 11 OF 13 HCAPLUS COPYRIGHT 2009 ACS on STN

AN 1995:728968 HCAPLUS Full-text
DN 123:129631
OREF 123:22754h,22755a
TI Semiconductor devices and manufacture thereof
IN Ohmi, Tadahiro; Yamada, Keiichi
PA Japan
SO PCT Int. Appl., 43 pp.
CODEN: PIXXD2
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9506329	A1	19950302	WO 1994-JP1373	19940819 <--
	W: US				
	RW: AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	JP 07122519	A	19950512	JP 1993-290786	19931119 <--
	JP 3688727	B2	20050831		
	EP 715343	A1	19960605	EP 1994-924391	19940819 <--
	R: CH, DE, FR, GB, IT, LI, NL				
PRAI	JP 1993-206741	A	19930820	<--	
	JP 1993-218889	A	19930902	<--	
	JP 1993-290786	A	19931119	<--	
	WO 1994-JP1373	W	19940819	<--	

AB A semiconductor device, suitable for use in ULSI, has a markedly reduced contact resistance between the electrode and the semiconductor layer and comprises an extremely shallow and thin contact structure. In the fabrication, ≥1 semiconductor and ≥1 metallic layer are formed continuously without exposing the laminate to the air and heat-treated for forming a compound therebetween, wherein the ion implantations are made before the heat treatment. In the contact structure, the depth to the interface between the compound and the semiconductor layer is < 22 nm. In the depth profile, a segment greater than a half of the compound is formed above the semiconductor layer. In the multilayer wiring structure, a thin silicide layer is formed in the contact segment connecting the upper and the lower metallic wirings.

IT 7440-48-4, Cobalt, uses
RL: DEV (Device component use); USES (Uses)
(interlayer circuit contact structures in ULSI)
RN 7440-48-4 HCAPLUS
CN Cobalt (CA INDEX NAME)

Co

IT 7803-62-5, Silicon hydride (SiH4), uses
RL: DEV (Device component use); RCT (Reactant); RACT (Reactant or reagent); USES (Uses)
(interlayer circuit contact structures in ULSI)
RN 7803-62-5 HCAPLUS
CN Silane (CA INDEX NAME)

SiH4

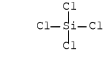
L104 ANSWER 12 OF 13 HCAPLUS COPYRIGHT 2009 ACS on STN

AN 1991:525147 HCAPLUS Full-text
DN 115:125147
OREF 115:21227a,21230a
TI Methods and apparatus for reactive ion etching
IN Gruenwald, Heinrich; Ramisch, Hans
PA Leybold A.-G., Germany
SO Ger. Offen., 12 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI DE 3935189	A1	19910508	DE 1989-3935189	19891023 <--
PRAI DE 1989-3935189		19891023 <--		

AB Methods for reactive ion etching of workpieces (especially of semiconductor substrates) entail the use of gas mixts. comprising Cl2, SiCl4, N2, and, optionally, AlCl3. Apparatus for carrying out the methods comprises a vacuum chamber containing upper and lower electrodes, the upper electrode being movable in relation to the lower electrode to allow it to be positioned to optimize the etching process.

IT 10026-04-7, Silicon tetrachloride
RL: USES (Uses)
(reactive ion etching using gas mixts. containing)
RN 10026-04-7 HCAPLUS
CN Silane, tetrachloro- (CA INDEX NAME)



IT 7440-48-4, Cobalt, reactions 12017-12-8, Cobalt disilicide
RL: RCT (Reactant); RACT (Reactant or reagent)
(selective reactive ion etching of, gas mixts. for)
RN 7440-48-4 HCAPLUS
CN Cobalt (CA INDEX NAME)

RN 12017-12-8 HCAPLUS
CN Cobalt silicide (CoSi2) (CA INDEX NAME)

RE.CNT 12 THERE ARE 12 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L104 ANSWER 13 OF 13 HCAPLUS COPYRIGHT 2009 ACS on STN
AN 1985:414543 HCAPLUS Full-text
DN 103:14543
OREF 103:2331a,2334a
TI Photoreceptor containing metal atoms and/or ions
IN Yamazaki, Toshinori; Sakai, Eiichi; Nomori, Hiroyuki
PA Konishiroku Photo Industry Co., Ltd. , Japan
SO Ger. Offen., 41 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

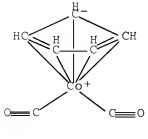
	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 3427637	A1	19850214	DE 1984-3427637	19840726 <--
	JP 60028658	A	19850213	JP 1983-137287	19830726 <--
	JP 60028659	A	19850213	JP 1983-137288	19830726 <--
	JP 60029469	A	19850214	JP 1983-137289	19830726 <--
	US 4668599	A	19870526	US 1986-896304	19860812 <--
PRAI	JP 1983-137287	A	19830726	<--	
	JP 1983-137288	A	19830726	<--	
	JP 1983-137289	A	19830726	<--	
	US 1984-634866	A1	19840725	<--	

AB Amorphous Si electrophotog. photoreceptors having improved resolution, tone, gradation, and image d. as well as better long-term stability in cyclic use contain a transition metal or metal ion which can act as a Friedl-Crafts catalyst. The photoreceptor is prepared by glow discharge decomposition in the presence of transition metal compds. Thus, a cylindrical Al support was coated with a an amorphous hydrogenated Si p-type blocking layer, an amorphous hydrogenated Si layer doped with B, and an amorphous hydrogenated Si layer containing 50-100 ppm Fe (by glow discharge of an Fe(CO)5/Ar/SiH4/B2H6 mixture). The resultant photoreceptor gave a high resolution, good color tone gradation, high d. and sharpness, and had an E1/2 value of 0.4 lx-s.

IT 7803-62-5, reactions 12078-25-0
RL: RCT (Reactant); RACT (Reactant or reagent)
(decomposition of, by glow discharge in amorphous hydrogenated silicon electrophotog. photoreceptor fabrication)

RN 7803-62-5 HCAPLUS
CN Silane (CA INDEX NAME)

RN 12078-25-0 HCAPLUS
CN Cobalt, dicarbonyl(η5-2,4-cyclopentadien-1-yl)- (CA INDEX NAME)



```
IT   7440-48-4, uses and miscellaneous
     RL: USES (Uses)
        (electrophotog. photoreceptor with photoconductive layer containing
        hydrogenated amorphous silicon and, with improved image quality)
RN   7440-48-4  HCAPLUS
CN   Cobalt  (CA INDEX NAME)


 Co


RE.CNT  2     THERE ARE 2 CITED REFERENCES AVAILABLE FOR THIS RECORD
              ALL CITATIONS AVAILABLE IN THE RE FORMAT


=> d his

     (FILE 'HOME' ENTERED AT 12:00:46 ON 09 MAR 2009)
               SET COST OFF

     FILE 'REGISTRY' ENTERED AT 12:00:52 ON 09 MAR 2009
               ACT AHMED575B/A
               ---------
L1   (        18)SEA FILE=REGISTRY SPE=ON  ABB=ON  PLU=ON  39517-09-4 OR 18839-3
L2   (         7)SEA FILE=REGISTRY SPE=ON  ABB=ON  PLU=ON  101753-14-4 OR 291-59
L3   (        25)SEA FILE=REGISTRY SPE=ON  ABB=ON  PLU=ON  (L1 OR L2)
L4   (         1)SEA FILE=REGISTRY SPE=ON  ABB=ON  PLU=ON  L3 AND C100H92SI9
L5   (         1)SEA FILE=REGISTRY SPE=ON  ABB=ON  PLU=ON  L3 AND C16H48SI8
L6   (        23)SEA FILE=REGISTRY SPE=ON  ABB=ON  PLU=ON  L3 NOT (L4 OR L5)
L7   (         1)SEA FILE=REGISTRY SPE=ON  ABB=ON  PLU=ON  NONASILANE/CN
L8   (         1)SEA FILE=REGISTRY SPE=ON  ABB=ON  PLU=ON  BR8SI3/MF
L9   (         1)SEA FILE=REGISTRY SPE=ON  ABB=ON  PLU=ON  "CYCLOTETRASILANE, SI
L10  (         1)SEA FILE=REGISTRY SPE=ON  ABB=ON  PLU=ON  "CYCLOTRISILANE, SILY
L11  (         1)SEA FILE=REGISTRY SPE=ON  ABB=ON  PLU=ON  CYCLOOCTASILANE/CN
L12  (         1)SEA FILE=REGISTRY SPE=ON  ABB=ON  PLU=ON  L6 AND SI4/ES
L13  (         2)SEA FILE=REGISTRY SPE=ON  ABB=ON  PLU=ON  4.859/RID AND 2/NR AN
L14  (         1)SEA FILE=REGISTRY SPE=ON  ABB=ON  PLU=ON  L13 AND 869812-46-4
L15  (         1)SEA FILE=REGISTRY SPE=ON  ABB=ON  PLU=ON  L6 AND SI7/ES
L16  (         1)SEA FILE=REGISTRY SPE=ON  ABB=ON  PLU=ON  "SPIRO(4.4)NONASILANE
L17          30 SEA FILE=REGISTRY SPE=ON  ABB=ON  PLU=ON  (L6 OR L7 OR L8 OR L9
               ---------

     FILE 'REGISTRY' ENTERED AT 12:02:25 ON 09 MAR 2009
L18           29 S L17 NOT 10026-04-7

     FILE 'HCAPLUS' ENTERED AT 12:03:39 ON 09 MAR 2009
L19         1763 S L18

     FILE 'REGISTRY' ENTERED AT 12:03:47 ON 09 MAR 2009

     FILE 'HCAPLUS' ENTERED AT 12:03:47 ON 09 MAR 2009
L20               TRA L19 1- RN :    10716 TERMS

     FILE 'REGISTRY' ENTERED AT 12:04:38 ON 09 MAR 2009
L21        10716 SEA L20
L22         1248 S SI/ELS AND H/ELS AND 2/ELC.SUB
L23          926 S L22 NOT (MAN OR TIS OR AYS OR PMS OR MXS OR CCS)/CI
L24          901 S L23 AND 1/NC
```

```
L25          182 S SI/ELS AND H/ELS AND CL/ELS AND 3/ELC.SUB AND 1/NC NOT  (MAN
L26          100 S SI/ELS AND H/ELS AND BR/ELS AND 3/ELC.SUB AND 1/NC NOT  (MAN
L27           66 S SI/ELS AND H/ELS AND I/ELS AND 3/ELC.SUB AND 1/NC NOT  (MAN O
L28          112 S SI/ELS AND H/ELS AND F/ELS AND 3/ELC.SUB AND 1/NC NOT  (MAN O
L29            9 S SI/ELS AND H/ELS AND CL/ELS AND BR/ELS AND 4/ELC.SUB NOT (MAN
L30           32 S SI/ELS AND H/ELS AND CL/ELS AND F/ELS AND 4/ELC.SUB NOT (MAN
L31            3 S SI/ELS AND H/ELS AND CL/ELS AND I/ELS AND 4/ELC.SUB NOT (MAN
L32            4 S SI/ELS AND H/ELS AND BR/ELS AND I/ELS AND 4/ELC.SUB NOT (MAN
L33           12 S SI/ELS AND H/ELS AND BR/ELS AND F/ELS AND 4/ELC.SUB NOT (MAN
L34            3 S SI/ELS AND H/ELS AND F/ELS AND I/ELS AND 4/ELC.SUB NOT (MAN O
L35            4 S SI/ELS AND H/ELS AND CL/ELS AND BR/ELS AND F/ELS AND 5/ELC.SU
L36            1 S SI/ELS AND H/ELS AND CL/ELS AND BR/ELS AND I/ELS AND 5/ELC.SU
L37         1624 S SI/ELS AND (CL OR BR OR F OR I)/ELS AND 1/NC NOT ((MAN OR TIS
L38         1889 S L17,L24-L37 NOT (C/ELS OR IUM OR (D OR T OR S OR B OR BI)/ELS
L39         1796 S L38 NOT (LI OR NA OR K OR RB OR CE OR BE OR MG OR CA OR SR OR
L40         1322 S L39 NOT (C OR GE OR SN OR PB OR N OR P OR AS OR SB OR BI OR O
                 E A/PG
L41         1319 S L40 NOT (E12 OR E21 OR E22)
                 SAV TEMP AHMED575C/A L41

     FILE 'HCAPLUS' ENTERED AT 12:16:54 ON 09 MAR 2009
L42        49612 S L41
L43        24112 S L42 AND PY<=2003 NOT P/DT
L44        17760 S L42 AND (PD<=20031016 OR PRD<=20031016 OR AD<=20031016) AND P
L45        41872 S L43,L44
                 E INTEGRATED CIRCUIT/CT
L46          394 S L45 AND E5-E15
                 E E5+ALL
L47          714 S L45 AND E7+OLD,NT
                 E E6+ALL
L48          324 S L45 AND E21+OLD,NT
L49         3713 S L45 AND E9+OLD,NT
L50         6344 S L45 AND H01L/IPC,IC,ICM,ICS,EPC
                 E GATE/CT
                 E E4+ALL
L51          209 S L45 AND E3
L52         7852 S L46-L51
L53         4907 S L52 AND ?FILM?
L54         1118 S L52 AND COAT?
                 E COATING/CT
L55          130 S L52 AND E12+OLD,NT
                 E COATLING MATERIALS,/CT
                 E COATING MATERIALS,/CT
                 E E11+ALL
L56          229 S L52 AND E8+OLD
L57         5290 S L53-L56
L58          327 S L57 AND LIGHT
                 E UV RADIATION/CT
L59           14 S L57 AND E3-E6
                 E E3+ALL
L60           36 S L57 AND E10+OLD,NT
L61            8 S L57 AND E29+OLD,NT
L62          758 S L57 AND HEAT?
                 E HEAT/CT
L63            0 S L57 AND E3+OLD,NT

     FILE 'REGISTRY' ENTERED AT 12:22:40 ON 09 MAR 2009

     FILE 'HCAPLUS' ENTERED AT 12:22:40 ON 09 MAR 2009
L64              TRA L57 1- RN :     4170 TERMS
```

```
     FILE 'REGISTRY' ENTERED AT 12:24:41 ON 09 MAR 2009
L65          4170 SEA L64
L66         13361 S L21,L65
L67           107 S L66 AND (CO/ELS OR ?COBALT?/CNS OR 7440-48-4/CRN)
L68            30 S L67 AND (AYS OR TIS)/CI
L69             2 S L68 AND SI/ELS AND 2/NC
L70            77 S L67 NOT L68
L71            35 S L70 NOT CCS/CI
L72             1 S L71 AND 1/ELC.SUB
L73            42 S L70 NOT L71
                  SEL RN 3-7 14 18-21 24 25 32 35
L74            28 S L73 NOT E1-E14

     FILE 'HCAPLUS' ENTERED AT 12:32:07 ON 09 MAR 2009
L75        213094 S L69,L72,L74
L76           380 S L75 AND L45
L77           100 S L76 AND L52
L78            77 S L77 AND L57
L79            16 S L78 AND L58-L62
L80            16 S L79 AND ?COBALT?
L81            75 S L78 AND ?COBALT?
L82             2 S L78 NOT L79,L81
L83             1 S L82 NOT PHOTORECEPTOR/TI
L84            76 S L79,L81,L83

     FILE 'REGISTRY' ENTERED AT 12:34:54 ON 09 MAR 2009

     FILE 'HCAPLUS' ENTERED AT 12:34:54 ON 09 MAR 2009
L85               TRA L84 1- RN :      483 TERMS

     FILE 'REGISTRY' ENTERED AT 12:34:57 ON 09 MAR 2009
L86           483 SEA L85
L87            53 S L86 AND (CO/ELS OR ?COBALT?/CNS OR 7440-48-4/CRN)
L88            16 S L87 AND (AYS OR TIS)/CI
L89             1 S L88 AND SI/ELS AND 2/ELC.SUB
L90            37 S L87 NOT L88
L91            11 S L90 NOT CCS/CI
L92             2 S L91 AND SI/ELS AND 2/ELC.SUB
L93            26 S L90 NOT L91
L94            24 S L93 NOT N/ELS

     FILE 'HCAPLUS' ENTERED AT 12:37:01 ON 09 MAR 2009
L95            28 S L89,L92,L94 AND L84
L96            24 S L77 NOT L84
                  SEL RN

     FILE 'REGISTRY' ENTERED AT 12:38:26 ON 09 MAR 2009
L97           300 S E15-E314
L98            26 S L97 AND (CO/ELS OR ?COBALT?/CNS OR 7440-48-4/CRN)
L99            11 S L98 NOT CCS/CI
L100            3 S L99 AND (CO/MF OR SI/ELS)
L101           15 S L98 NOT L99
L102           14 S L101 NOT N/ELS

     FILE 'HCAPLUS' ENTERED AT 12:40:22 ON 09 MAR 2009
L103           24 S L100,L102 AND L96
                  SEL AN 3 5 7 10-13 18 20 21 23
L104           13 S L103 NOT E315-E336
```

=>